Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

SECOND SEMESTER M.TECH (OP. ELECTIVE) DEGREE END SEMESTER EXAMINATION - APRIL / MAY 2017

SUBJECT: ARM PROCESSOR AND APPLICATIONS (ECE - 5233)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Explain AMBA based system emphasizing on bus transfers, slave, APB, AHB and ARM multiplexed bus scheme.

1B. LEDs are connected to each pins starting from P1.16 to P1.23 in an ARM state LPC 2129 target board. Write an ALP to turn ON and OFF one by one with a maximum possible time delay in between. Repeat the sequence.

1C. Discuss ARM address register structure.

(4+4+2)

2A. With block diagram, describe how an ARM core is used in an Ericsson –VLSI blue tooth base band controller?

2B. How are stack operations carried out in the ARM processor when it is in ARM state.?
Tabulate all the addressing modes and explain with an example.

2C. Explain Interrupt I/O strategy with algorithm / program used for implementation.

(4+4+2)

3A. Sketch block diagram of ARM core data flow model and describe the following.

i) Barrel Shifter
ii) CPSR
iii) Register set

3B. Write an ALP using ARM Thumb state instructions to add two 64 bit numbers stored in memory locations pointed by registers r0 and r1. Store the sum in memory location pointed by register r0.

3C. What are the different data types ARM supports in high level languages? Explain.

(4+4+2)

4A. With examples, explain direct mapped and set associative mapped cache memory systems with examples. Discuss limitations of these mapping schemes.

4B. What are the different types of logical instructions in ARM? Explain each one with an example.

4C. Discuss physical features of ARM design philosophy.

(4+4+2)

5A. Discuss different factors affecting cache optimization and solutions to overcome them.

5B. With regard to ARM MMU, explain the following components with necessary diagrams.

i) Different types of page tables.

ii) Different page table entries

Virtual address issued = 11111111111011111111000000001111 (FFEFF00F)

i) Single step page table walk.

ii) Two step page table walk with L2 coarse table.

5C. Given data: 0x 12345678. How this data can be separately stored in a little and big endian memory. Show with a sketch. Mention one application of each memory storage method.

(4+4+2)