Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

SECOND SEMESTER M.TECH (MICROELECTRONICS)
DEGREE END SEMESTER EXAMINATION – APRIL / MAY 2017
SUBJECT: CMOS MIXED SIGNAL DESIGN (ECE- 5222)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Give OTA-C current-mode Tow-Thomas[TT] biquad circuit and derive expressions for two current-in current-output transfer functions. Give the expression for pole frequency and pole-Q.

1B. Give the basic three op-amp based TT biquad. What is a Deboo integrator? Give the circuit of TT biquad using two op-amps?

1C. Define the following terms: [i] Dynamic range [ii] Total Harmonic Distortion (THD)

(5+3+2)

2A. With a schematic circuit explain the working of 4-bit charge scaling DAC. Discuss the layout considerations for the capacitor array used in charge scaling DAC.

2B. How Miller's theorem can be employed to realize negative capacitance circuit using OTA?

2C. Give fully differential G_m-C realization of floating inductor as series element.

(5+3+2)

3A. Give the g_m-C current-mode realisation of RLC parallel resonator circuit shown in **FIG. Q3A**. Derive the expressions for different transfer functions. Give your comments.

3B. Find the transfer function of the circuit in **FIG. Q3B** and give your comments.

3C. Give the op-amp based circuit for simulating grounded negative impedance with the expression for input impedence.

(5+3+2)

4A. [i] Give the circuit of OTA-C current-mode third-order canonical all-pole filter. Derive the expression for transfer function.

[ii] With the schematic circuit explain the comb filter realization.

4B. Explain the practical OTA macro models.

4C. State how the resolution of ADC can be enhanced without using an external ADC.

(5+3+2)

5A. Discuss the design methods and layout guidelines employed in Analog and Mixed-Signal Circuit Design with respect to following: [i] Power supply and grounding issues [ii] Guard Rings [iii] Shielding

5B. Discuss the linearity related errors as applicable to DACs.

5C. [i] Show how current conveyor CCII- may be viewed as MOS transistor.
[ii] Show CCII can be used as VCCS.

(5+3+2)

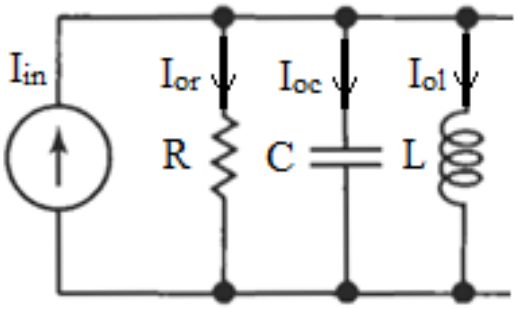

FIG. Q3A

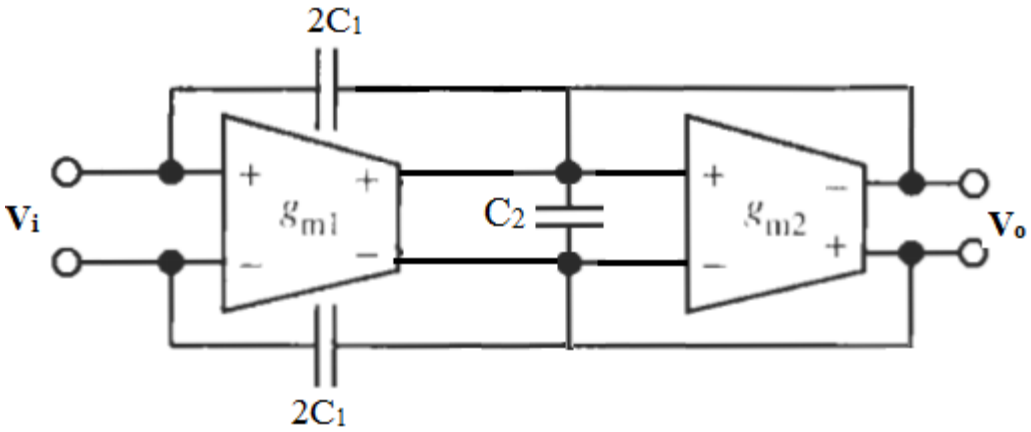

FIG. Q3B