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## MANIPAL INSTITUTE OF TECHNOLOGY Manipal University SECOND SEMESTER M.TECH (DEAC/MICROELECTRONICS) DEGREE END SEMESTER EXAMINATION – APRIL / MAY 2017 SUBJECT: CAD TOOLS FOR VLSI DESIGN (ECE-5234)

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MAX. MARKS: 50

Instructions to candidates

- Answer ALL questions.Missing data may be suitably assumed.
- 1A. Find complement of the following function using Recursive algorithm F=wx'y+w'xy+yz'+wxy'z'
- 1B. Determine the prime implicants for the following function using iterated consensus method F=x'z'+xyz'+xy'z'+xy'z
- 1C. Explain heuristic minimization. What are all the different types of heuristic minimizers available

(5+3+2)

2A. Find the essential prime implicant for the set of prime implicants  $F = \{C_1, C_2, C_3, C_4\}$  where

 $C_1=x_1$ ' $x_3$ ' $x_4$ '  $C_2=x_1x_2$   $C_3=x_3x_4$   $C_4=x_2x_3$ ' $x_4$ ' using ESPRESSO algorithm.

2B. Find the test vector to test single stuck at faults for the circuit shown in Fig.Q2B using Boolean difference method.

(5+3+2)

- 3A. Apply Hu algorithm for the given data flow graph shown in Fig.Q3A. Assume  $\gamma=4$ , P(0)=1,P(1)=3,P(2)=4,P(3)=2,P(4)=2. Determine the resource constraints. Draw the scheduled graph with resource constraints
- 3B. Explain ALAP algorithm
- 3C. Draw the stick diagram for the function F=(A'B+AB')'

(5+3+2)

- 4A. Find the test vector using Iterative test generator for the circuit shown in Fig.Q4A
- 4B. Find the sequence for the faulty and fault free circuit using signature analysis technique to test the single stuck at faults ( $\alpha$  at SA<sub>0</sub>,  $\beta$  at SA<sub>1</sub>) shown in Fig.Q4B. Assume it's a 4 bit shift register and the third bit from MSB is connected as feedback to the one input of XOR gate.
- 4C. Find the collapse ratio for the given circuit shown in Fig.Q4C

(5+3+2)

<sup>2</sup>C. Explain Y chart

- 5A. Implement full adder using 2 half adders and 1 OR gate using ACT3 logic module. Determine the number of logic modules required to implement.
- 5B. Implement F=a'cd+b'cd+a'b+bc' using 4\*2\*1 Altera max FPGA (use shared logic expander)
- 5C. Draw ROBDD for the function F=ab+bc+ca in the order of a-c-b

$$(5+3+2)$$



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