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MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

SECOND SEMESTER M.TECH DEGREE END SEMESTER EXAMINATION - APRIL / MAY 2017
SUBJECT: EMBEDDED SYSTEM DESIGN (ECE - 5242)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. List the available processor technologies. The state diagram of a control unit is shown in FIGURE Q1A. Z, Q_1, Q_0 are the inputs. Design the control unit using suitable counter, decoder and sequence controller.

1B. Define the following terms.
(a) Reliability (b) Portability (c) Time to market.

1C. The NRE cost involved in designing an embedded product is $500. The total cost involved in designing 100 units is $10500. Calculate per unit cost.

(5+3+2)

2A. The connection of devices to 8051 MC is given in Table Q2A. Write an embedded C program to display 'A' on the seven segment display and rotate the motor anticlockwise when the switch is not pressed and display 'C' on the seven segment display and rotate the motor clockwise when the switch is pressed. Assume that switch provides a logic LOW to the controller.

TABLE Q2A

Device	8051 Connection
Stepper motor	P1.0-P1.3
Common anode Seven segment display	Port 2
Switch	P3.1

2B. Explain the following:
(a) SPI (b) Memory shadowing (c) Brown-out protection circuit.

2C. Draw the DFG for the following equations:
$x1 = a + b; y = a \times c; z = x1 + d; x2 = y - d; x3 = x2 + c$

(5+3+2)

3A. Consider a case where process ID's P1, P2, P3 with estimated completion time 10, 8, 3 milliseconds is supposed to enter the ready queue together in the order P2, P3, P1. Process P4 with estimated execution completion time 4 milliseconds will enter the ready queue after 6 milliseconds. Which scheduling algorithm (LIFO or FIFO) is suitable for the given case?

3B. Differentiate between the following:
(a) Process and thread
(b) Types of kernels
(c) Types of RTOS.
(d)

3C. What are the functions of the following development tools?
(a) Cross compilers (b) Emulators

(5+3+2)

4A. Draw the internal block diagram of ARM processor and explain the following.
(a) Register file (b) Load store architecture (c) Conditional execution

4B. Given r3=0x04 and r5=0x0B. What would be the contents of registers in each of the following cases after the Thumb instruction is executed.

(a) SUB r3,r5 (b) CMP r3,r5 (c) MVN r3,r5

(e) NEG r3,r5 (e) AND r3,r5 (f) TST r3,r5

4C. Differentiate between AHB and ASB.

(5+3+2)

5A. With a neat diagram explain the different phases of EDLC.

5B. With a neat diagram explain the JTAG based boundary scanning for hardware testing.

5C. List the different power reduction techniques used in designing low power embedded systems.

(5+3+2)

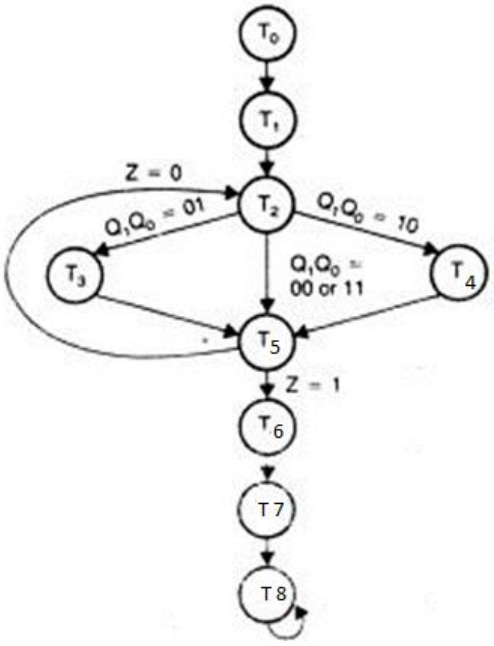

FIGURE Q1A