Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

FIRST SEMESTER M.TECH (E & C) DEGREE END SEMESTER EXAMINATION - APRIL / MAY 2017
SUBJECT: LOW POWER VLSI DESIGN (ECE – 5221)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Explain the concepts of parallelism and pipelining in architecture to minimize the power dissipation and compare them.

1B. Discuss i) Clock gating and ii) Pre-computation for low power and show how it can be implemented at RTL level using HDL code.

1C. List the problems faced when level converters are used to support dual V_{DD} technique in CMOS circuits. (5+3+2)

2A. Explain any two methods each for reducing the switching activity in the circuit and bus, for lowering dynamic power dissipation.

2B. Explain with suitable illustrations the following techniques employed in coding for low power: i) Loop unrolling ii) Operation Reduction

2C. Estimate the switching activity at the output of a logic circuit implemented using basic gates for the Boolean expression Y= (A+B)C. Assume P(A) = 0.3, P(B) = 0.4, P(C) = 0.3. (5+3+2)

3A. Explain dual Vth and variable Vth techniques employed for leakage reduction in CMOS circuits and compare them.

3B. Discuss process level techniques employed for reducing leakage in MOSFETs.

3C. List the salient features of short circuit power in CMOS circuits. (5+3+2)

4A. Explain i) Power gating and ii) Gate length biasing for reducing leakage power in CMOS circuits.

4B. Discuss crosstalk in VLSI circuits and it's impact on the power dissipation. Also explain the techniques used to minimise crosstalk.

4C. What is the impact of using repeaters in interconnects? Explain. (5+3+2)

5A. Identify at least 5 basic components of a laptop from the point of view of power management and describe the techniques that can be applied for power reduction. Justify your choice.

5B. Explain with suitable expressions the basic principle of Adiabatic switching and discuss the challenges in implementation of adiabatic circuits.

5C. Compare Task Based and Device level Power Management techniques employed at the OS level.

(5+3+2)