Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
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SECOND SEMESTER M.Tech. DEGREE END SEMESTER EXAMINATION - April/May 2017

SUBJECT: System on Chip Design (ECE - 5256)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Assume the features of an embedded system are given in the form of technical tasks *T0, T1, T2, T3, T4* and *T5*.

i. Explain the concept of application mapping and activity scheduling in a typical embedded system design flow.

ii. Map the application shown as task graph in **Fig.1.1** to suitable processing elements given in **Table.1.1** to finish the whole execution before 15 msec. (multiple instances of same processing element is not allowed).

iii. Draw the activity scheduling graph for the application mapped in above question.

Task	CPU1	CPU2	ASIC
	T(ms)	*T(ms)*	*T(ms)*
T0	2	3	1
T1	2	4	6
T2	4	3	8
T3	4	9	5
T4	6	8	5
T5	8	6	9
$\gamma_{0,1} = \gamma_{0,2} = \gamma_{2,4} = \gamma_{3,5} = 1$ ms			

T(ms)*-Time taken by each task to execute(in milli seconds).*

Table 1.1

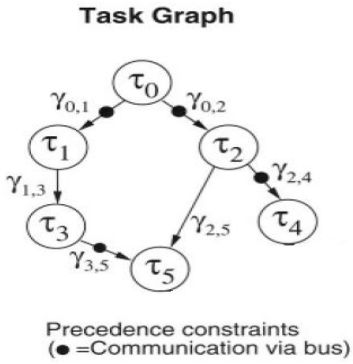

Fig.1.1

1B. Write the special features of digital signal processor should have over other data processing elements.

1C. List out the design challenges of an SoC.

(5+3+2)

2A. Write differences among the following

i. MicroBlaze processor and ARM cortex-A9 processor

ii. Executable linkable format file and Bit file

iii. ASIC and FPGA

iv. General Purpose processor and Digital Signal processor

v. Zynq SoC and Programmable SoC

2B. Explain Hardware and Software co-synthesis in system level design flow.

2C. An young engineer is in confusion of selecting proper processing element to implement the following operation:

$E = A \; X \; B,$

$F = C \div D,$

$G = E + F$ *[where A,B,C,D,E,F are registers of appropriate size]*

If high speed & low cost are his primary objectives then which one you suggest among GPP, FPGA and ZYNQ SoC to get optimum solution. Give reason.

(5+3+2)

3A. Write and explain the design rules of RISC philosophy

3B. Design an automatic tea/coffee vending machine based on FSM model for the following requirement: The tea/coffee vending is initiated by user inserting a 5 rupee coin. After inserting the coin, the user can either select 'Coffee' or 'Tea' or press 'Cancel' to cancel the order and take back the coin.

3C. Explain AHB and APB buses of AMBA

(5+3+2)

4A. Write & Implement the cycle conserving DVS algorithm for EDF scheduler on the task set given in **Table 4.1** and **4.2**. Explain it by drawing scheduling graph.

Task	Computing time	period
1	3ms	8ms
2	3ms	10ms
3	1ms	14ms

Table 4.1: computing times are specified at the maximum processor frequency

Task	Invocation 1	Invocation 2
1	2ms	1ms
2	1ms	1ms
3	1ms	1ms

Table 4.2: Actual computation requirement of the task set (assuming execution at maximum frequency)

4B. For the task set given in **Table 4.3**, find the CPU utilization and find out whether it is schedulable using the RM algorithm. Draw the scheduling graph.

Tasks	Period	CPU Burst	Release Time
T1	3	1	0
T2	10	3	1
T3	15	4	3

Table 4.3

4C. Explain the problem of stack overflow that occurs during nested exceptions, give the solution that helps in overcoming it.

(5+3+2)

5A. What is LEDES algorithm? Write and explain it in detail.

5B. In OS based embedded software implementation, draw and explain the interrupt timing diagram to process I/O request once an interrupt arises.

5C. List out the drawbacks that need to be taken into account while lowering supply voltage Vdd to reduce energy dissipation for SoC

(5+3+2)