Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

SECOND SEMESTER M.TECH (ME/DEAC) E & C DEGREE END SEMESTER EXAMINATION (APRIL/MAY 2017)
SUBJECT: VLSI PHYSICAL DESIGN AND VERIFICATION (ECE - 5258)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer ALL questions.
- Missing data may be suitably assumed.

1A. For the circuit shown in Fig. 1A, assume a unit delay through the Register and Logic blocks (i.e., $t_R = t_L = 1$). Assume that the registers, which are positive edge triggered, have a set up time t_S of 1 and the delay through the multiplexer t_M equals $2t_R$.
   i) Determine the minimum clock period disregarding the clock skew.
   ii) Repeat part (a), factoring in a nonzero clock skew: $\delta = t'_\theta - t_\theta = 1$.
   iii) Repeat part (a), factoring in a non-zero clock skew: $\delta = t'_\theta - t_\theta = 4$
   iv) Derive the maximum positive clock skew that can be tolerated before the circuit fails.

1B. Derive the expression and calculate the delay of each 6-input AND gate as shown in Fig. 1B using logical effort (LE) method. Which design is fastest for electrical effort (H) = 1, 5, and 20?

(5+5)

2A. Draw the Gajski's Y-chart and illustrates the Top-Down design methodology?

2B. Explain the top level design flow and each file format used in prime time tool for Static Timing Analysis (STA). How does the prime time analyse a design over various Temperature (T), Voltage (V) and Process variations?

2C. A balanced clock distribution scheme has been shown in Fig. 2C. For each source of variation, identify the sources of skew and jitter at the position 1, 2, 3, 4, 5 and 6.

(2+5+3)

3A. The five-pin net with pins a, b, c, d and e has been shown in Fig. 3A. Do the following,
   (a) Draw a monotone chain model, a rectilinear minimum spanning (RMST) tree and a rectilinear steiner minimum tree (RSMT) to connect all the pins.
   (b) Find the weighted total wire-length using each estimation technique from (a) if each grid edge has unit length and weight is 2.

3B. Realize a PROM of the smallest appropriate size by drawing the logic diagram in PLD notations of the LUT corresponding to the decimal arithmetic expression $F(X) = 2X + 4$ for $0 \leq X \leq 7$, where $F(X)$ and X are expressed in binary.

(5+5)

4A. Briefly explain the major problems of Integer Linear Floor planning (ILP) and formulate the ILP for the following problem instances by assuming the desired aspect ratio (= width/height) is 1, when rotation is not allowed. The dimension of four modules are given as (width (W), height (H)): $m1$ (2, 5), $m2$ (3, 6), $m3$ (7, 4), and $m4$ (6, 6). Assume the width (W) is fixed, and possible objective is to minimize the height (H) of the floorplan.

4B. Briefly explain the simulation based verification methodology using block diagram? What are the coverage matrices?

(6+4)

5A. What are the major components of a simulator? Briefly explain event driven simulator and how the timing wheel mange them? What are the five layers of events and their order of execution taken in Verilog IEEE standards? Consider a piece of code given below and find the order of execution.

```
always @(posedge clock)
    begin
    x = a;
    end
always @(posedge clock)
    begin
    x = b;
    y <= x;
    y = c;
    end
```

5B. Perform the pin assignment using topological nine zone method as shown in Fig. 5B?

5C. Briefly explain the basic principle of design verification using block diagram.

(5+2+3)

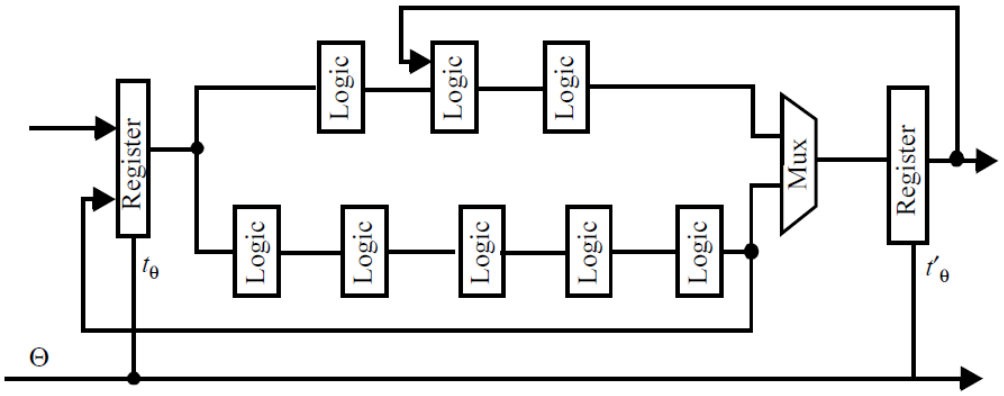

Figure 1A

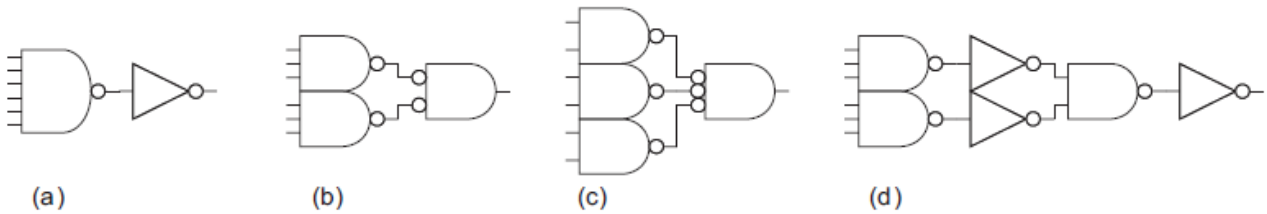

Figure 1B

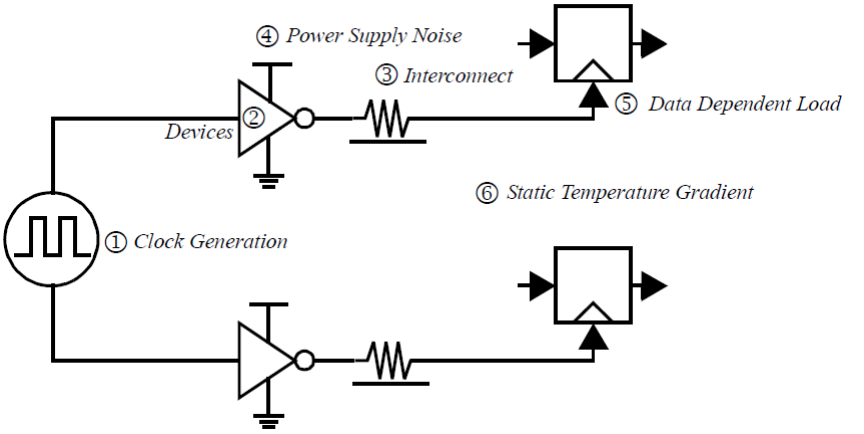

Figure 2C

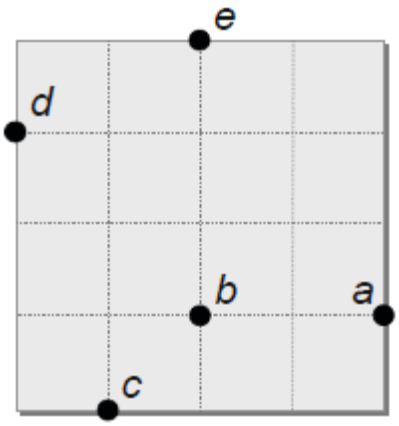

Figure 3A

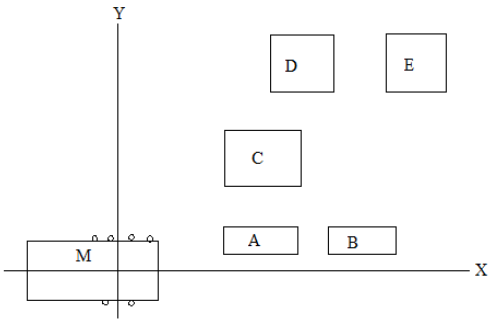

Figure 5B