Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

II SEMESTER M.TECH (ESM/PED) END SEMESTER EXAMINATIONS, APRIL - MAY 2017

SUBJECT: DESIGN OF DIGITAL SYSTEMS [ELE 5234]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 25, April 2017** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. A given system has four sensors that can produce an output of 0 or 1. The system operates properly when exactly one of the sensors has its output equal to 1. An alarm must be raised when two or more sensors have the output of 1. Design the simplest circuit that can be used to raise the alarm. Implement the circuit using 4:1 multiplexers and residual gates. ***(03)***

1B. A logic circuit has two inputs, *Clock* and *Start*, and two outputs, *f* and *g*. The behavior of the circuit is described by the timing diagram in Figure 1B. When a pulse is received on the *Start* input, the circuit produces pulses on the *f* and *g* outputs as shown in the timing diagram Figure 1B. Design a suitable circuit using only the following components: a three bit resettable positive-edge-triggered synchronous counter block and basic logic gates. For your answer assume that the delays through all logic gates and the counter are negligible. ***(02)***

1C. Write Verilog HDL code for 8:1 multiplexer using 2:1 multiplexer as a component. ***(05)***

2A. Draw the state diagram to count the number of '@' character [ASCII code is 40H] in blocks of 256 characters. Each character is represented by an 8 bit ASCII code ***(04)***

2B. Draw the state diagram for the serial adder shown in Figure 2B. ***(03)***

2C. For the circuit shown in Figure 2C write the behavioral Verilog HDL code. ***(03)***

3A. Write a Verilog HDL program to detect the non-overlapping sequence "1010". Use Moore type FSM. ***(06)***

3B. Write a sequential Verilog HDL program for finding the greatest of 3 numbers using Function or Task. ***(04)***

4A. Develop a counting system to count the number of people inside the museum. Sensors present at the entrance and exit door of the museum produce an output of 1 when a person enters or leaves the museum. Museum has the maximum capacity of accommodating people at a time is 100. If the number of people inside the museum is 100, entrance door of museum should be closed. Write the Verilog HDL code to implement the same. ***(05)***

4B. Design 8 bit universal type shift register to do the following operations. Write the Verilog HDL code.

S2	S1	S0	Operations
0	0	0	Reset to Zero
0	0	1	Parallel Load
0	1	0	Increment
0	1	1	Decrement
1	0	0	Shift left
1	0	1	Shift Right
Others			No operation

(05)

5A. Write the short notes on following

i. Antifuse

ii. SRAM Programming Technology ***(04)***

5B. Show how a 12 input AND gate can be implemented using Xilinx SPARTAN-IIE CLB ***(02)***

5C. Sketch the basic block diagram of Xilinx **Spartan IIE** FPGA and briefly explain the major configurable elements. ***(04)***

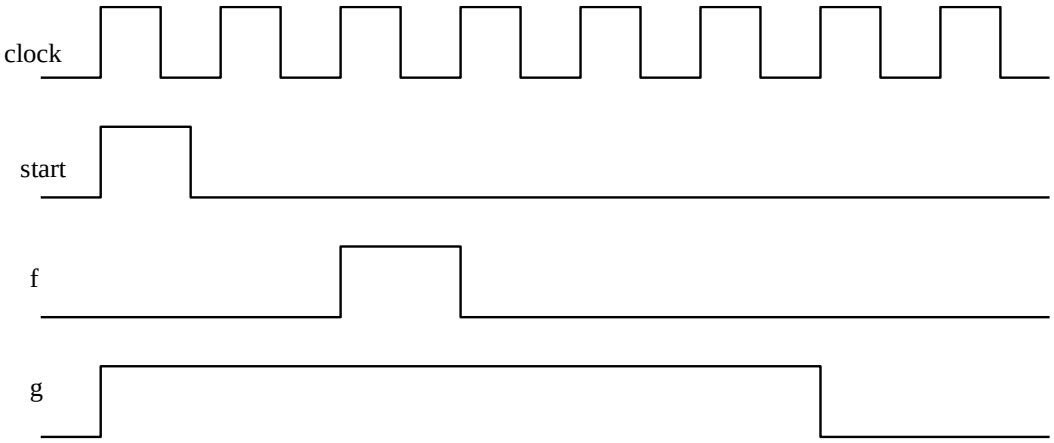

Figure 1B

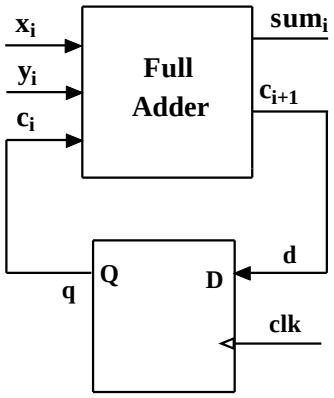

Figure 2B

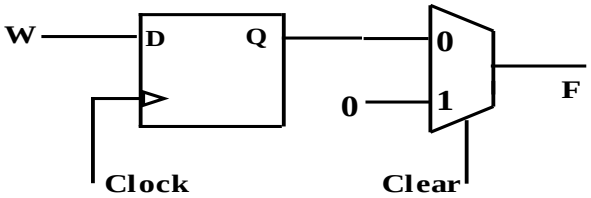

Figure 2C