Question Paper



MANIPAL UNIVERSITY

SCHOOL OF INFORMATION SCIENCES (SOIS) FIRST SEMESTER MASTER OF ENGINEERING - ME (EMBEDDED SYSTEMS) DEGREE EXAMINATION - APRIL 2017 Saturday, 22,2017 Time:10:00AM-1:00PM

Advanced Computer Architecture [ESD 611]

Marks: 100 Duration: 180 mins.

Answer all the questions.

- A) Write a short note on Harvard Architecture (10) of the computer
 - B) Compare CISC and RISC machines
- The instruction set of a computer consists of the following instructions with relative frequencies.

LOAD 1/2 STORE 1/8 ADD 1/8 AND 1/8 NOT 1/32 RSHIFT 1/32 JUMP 1/32 HALT 1/32

Encode these instructions using Huffmanâ \in [™]s method. Calculate the redundancy introduced by this scheme.

- Explain the implementation of a 4-bit carry look ahead circuit using which construct a 4 bit carry look ahead circuit and comment on the computation time.
- 4) Explain the division using restoring algorithm (10) with the flowchart and show 13/5

Consider the following register transfer description. (10)

Declare registers M [4], Q [3], S [7], J [3];

Declare bus Outbus [7]:

Declare bus Outbus [7]; Start: $M \leftarrow 14, Q \leftarrow 5, S \leftarrow 0$;

Loop1: If M = 0 then go to Halt;

J=1:

Loop2: If J > Q then go to Dec;

$$S \leftarrow S + 1;$$

 $J \leftarrow J + 1$;

Outbus ← S;

Go to Loop2;

Dec: $M \leftarrow M - 1$;

Go to Loop1

Halt: End

Design a hardwired controller that will implement this algorithm.

Using a 4-bit parallel adder with inputs A, B, and C_{in} , outputs F and C_{out} and one select line S_o design an arithmetic circuit - as follows.

 S_0 F

7)

0 A plus B

1 B plus 1

Using another select line S_1 , modify the above circuit to carry out a 4 function ALU whose truth table as given below.

$$S_1$$
 S_0 F

0 0 A plus B
0 1 B
1 0 shift left A
1 1 NOT A

Explain the seven different operating modes of (10)

	ARM7	
8)	Explain the Data Processing Instruction execution in ARM7	(10)
9)	Explain the Barrel shifter in ARM7 with relevant examples	(10)

Explain data hazards and instruction hazards in pipelining process (10)