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## MANIPAL UNIVERSITY

## SCHOOL OF INFORMATION SCIENCES SECOND SEMESTER MASTER OF ENGINEEING - ME(EMBEDDED SYSTEMS) DEGREE MAKE-UP EXAMINATION - JULY 2017 Monday, 10 July, 2017 Time: 10:00 to 13:00

## Digital Signal Processing [ESD 602]

A

Marks: 100

Duration: 180 mins.

## Answer all the questions.

1) Compute the DFT of the sequence x(n) = [1, -1, -1, -1, 1, 1, 1, (10)]1, -1] using DIT-FFT algorithm. Draw the flow graph indicating the intermediate values 2) (10)Realize the following system function using Direct form-I, Direct form-II and Cascade / Parallel forms  $H(z) = [(z^2 + 0.5z + 1)(z + 0.6)] / [(z^2 + 0.6z + 0.2)(z - 1)(z + 0.6)] / [(z^2 + 0.6z + 0.6)(z - 1)(z + 0.6)] / [(z^2 + 0.6z + 0.6)(z - 1)(z + 0.6)] / [(z^2 + 0.6z + 0.6)(z - 1)(z + 0.6)] / [(z^2 + 0.6)(z + 0$ 0.8)] 3) (10)Design an ideal linear phase FIR low pass filter with a cutoff frequency of  $\pi/2$  radians, using frequency sampling technique. Assume 11 tap coefficients (10)4) It is desired to remove low frequencies of an analog signal with a digital linear phase FIR filter. The 3 dB frequency is 2 KHz, transition width is 500 Hz and the stop band attenuation is 50 dB. Use suitable window function to design the filter to meet the above specification. The filter employs a sampling frequency of 10 KHz. 5) A third ordered Chebychev lowpass filter with 3 dB frequency (20) of 5 KHz is to be realized using digital system. The sampling period is 10  $\mu$ sec. Realize the filter using Impulse Invariance technique

10/07/2017	Question Paper	
6)	Provide polyphase filter structures of interpolator and	(10)
	decimator. Explain how these structures are in a position to provide the required sampling rate conversion	0
7)	What is a digital filter bank? Explain how an uniform DFT filter bank can be implemented using multirate signal processing	(10)
8)	Explain LMS adaptive algorithm. Explain how LMS adaptive algorithm is made use to make the Weiner Filter Configuration adaptive based on the steepest descent technique	(10)
9)	Explain the internal and external memory organization in TMS320C6X DSP Processor	(10)
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