MANIPAL UNIVERSITY

SCHOOL OF INFORMATION SCIENCES (SOIS)
SECOND SEMESTER MASTER OF ENGINEERING - ME (EMBEDDED SYSTEMS / FOURTH SEMESTER MSc Tech(VLSI DESIGN / EMBEDDED SYSTEMS)
DEGREE EXAMINATION - APRIL / MAY 2017
Wednesday, 19, 2017
Time : 10:00 AM - 1:00 PM

Digital Signal Processing [ESD 602]

Marks: 100 **Duration: 180 mins.**

A

Answer all the questions.

1) Find the DFT of x(n) = [1, 2, 3, 4, 4, 3, 2, 1] using DIF-FFT algorithm (10)

2) Realize the following system function using Direct form-I, Direct form-II and Cascade / Parallel forms (10)

$$H(z) = [2(1-z^{-1})(1+1.414z^{-1}+z^{-2}) / [(1+0.5z^{-1})(1-0.9z^{-1}+0.81z^{-2})]$$

3) Design a linear phase bandpass FIR filter having cut-off frequencies of 1 KHz and 3 KHz using Frequency Sampling Technique. The system employs a sampling frequency of 8 KHz. Assume 10 tap coefficients. (10)

4) Design an FIR linear phase lowpass filter using windows to meet the following specifications. (10)

$$0.99 < |H(e^{jw})| \leq 1.01; \quad \text{for} \quad 0 \leq |w| \leq 0.19\pi \text{ rads}$$

$$|H(e^{jw})| \leq 0.01; \quad \text{for } 0.21\pi \leq |w| \leq \pi \text{ rads}$$

5) Design using impulse invariance technique, a digital Butterworth lowpass filter for the following specifications. (20)

$$|H(j\Omega)| \geq -1 \text{ dB} \qquad 0 \leq \Omega \leq 100 \text{ rad/sec}$$

$$|H(j\Omega)| \leq -40 \text{ dB} \qquad \Omega \geq 2000 \text{ rad/sec.}$$

Sampling frequency = 8000 rad/sec. Realize the filter structure.

6) Provide polyphase filter structures of interpolator and decimator. Explain how these structures are in a position to provide the required sampling rate conversion (10)

7) (10)

Explain how multirate signal processing can be used in the analysis and synthesis of sub-band coding of speech signals.

8) Explain analytically, how optimum filter coefficients are obtained on Mean Square Error sense in Wiener Filter Configuration. (10)

9) Draw the architecture of a TMS320C6X DSP processor and give the functionality of each of the block. (10)