**Question Paper** 



## MANIPAL UNIVERSITY

## SCHOOL OF INFORMATION SCIENCES SECOND SEMESTER MSc INFORMATION SCIENCE DEGREE MAKE - UP EXAMINATION - JULY 2017 Friday, 14 July, 2017 Time: 10:00 to 13:00

**Computer Architecture - Elective 1 [MIS 510.2]** 

Marks: 100

Duration: 180 mins.

## Answer all the questions. <u>All questions carry equal marks</u>

| 1) | Explain with a block diagram a Accumulator based machine  | (10) |
|----|---|------|
| 2) | In a computer instruction format, the<br>instruction length & size of the address field<br>are 11 & 4 respectively. If the number of 2<br>address instructions are 5, calculate the<br>possible combinations of one & zero address<br>instructions. | (10) |
| 3) | The instruction set of a computer consists of six (6) instructions $I_0$ , $I_1$ , $\hat{a} \in \{, I_5\}$ . The relative frequency of these instructions are as follows $(6+2+2)$ marks  | (10) |

(6+2+2) marks

| l <sub>0</sub> | $I_1$ | l <sub>2</sub> | l <sub>3</sub> | I <sub>4</sub> | l5   |
|----------------|-------|----------------|----------------|----------------|------|
| 1/2            | 1/4   | 1/16           | 1/16           | 1/16           | 1/16 |

a) Encode these instructions using Huffman's method

b) Calculate the total number of bits saved compared to block encoding method

c) Calculate the average number of bits per instruction.

4)

(a) Design a combinational circuit with 3 inputs & one output. The output is "1" when (10)

|     | the input binary value is less than 5 & is "0"<br>otherwise. (5<br>marks)  |     |
|-----|--|-----|
|     | (b) Design a combinational circuit for the<br>following specifications: $Y = 1$ , if A is 1 or B and<br>C are 1, Z= 1, if B or C is 1 but not<br>both. (5<br>marks)  |     |
| 5)  | Write a circuit of a 4 bit two input Carry look (10)<br>ahead Adder (CLA) and compare its execution<br>speed with 4 bit two input Carry Propagate<br>Adder.  | ))  |
| 6)  | Design a four bit two input ALU unit to (10<br>implement ADD, SUB, NOT & NAND functions.   | ))  |
| 7)  | Design a microprogrammed control unit to (10<br>multiply two 4 bit numbers using Booth's<br>multiplier.  | ))  |
| 8)  | Explain (a) Direct (b) Fully Associative mapping <sup>(10)</sup><br>policies with suitable block diagram. Compare<br>the advantages and disadvantages of<br>both (4+4+2)<br>marks  | ))  |
| 9)  | Assume a main memory has 3 page frames (10<br>and initially all page frames are empty.<br>Consider the following stream of references  | ))  |
| 10) | 2,3,2,4,6,2,5,6,1,4,6<br>Calculate the hit ratio if the replacement policy<br>used is<br>FIFO (b) LRU (c) Optimal replacement<br>policy. $(3+3+4)$<br>marks<br>The size of the virtual address space = 8 k <sup>(10)</sup> | 0)  |
|     | words<br>Size of the physical address space = 2k words.  | - , |
|     | Page size = 512 words  |     |
|     | The page request sequence is:  |     |

0,1,2,3,5,6,3,4,7,2,6,5.

a. Calculate the number of physical & virtual pages (2 marks)
b. Calculate value of "h" for the above sequence in case of Direct mapping (4 marks)
c. Find all the virtual addresses that generate page fault after the end of the above

sequence. (4 marks)