

**MANIPAL
UNIVERSITY**

Question Paper

28-Apr-2017 11:22:16
TECHNICAL SUPPORT[Support](#) | [Change Password](#) | [Logout](#)[Basic Masters](#)[Question Paper](#)[Device & Dockets](#)[Evaluation](#)[Evaluation Reports](#)[Reports](#)[Utilities](#)Select Exam Event SOIS End Semester April 2017 ▼☐ Show answer keys for MCQ.[Back](#)

MANIPAL UNIVERSITY

SCHOOL OF INFORMATION SCIENCES (SOIS)
SECOND SEMESTER MASTER OF SCIENCE - M.Sc. (INFORMATION SCIENCE)
DEGREE EXAMINATION - APRIL 2017
Friday, 28,2017
Time :10:00AM- 1:00PM

Computer Architecture - Elective 1 [MIS 510.2]

Marks: 100

Duration: 180 mins.

A

Answer all the questions.

- 1) Bring out the relevance of Computer Architecture design in terms of: (10)
 - a) Hardware functional units
 - b) Size of the memory
 - c) Programming languages used (3+4+3) marks
- 2) Design a computer system for ADD, SUB, MUL and DIV operations. (10)
- 3) In a computer instruction format, the instruction length & size of the address field are 8 & 3 respectively. If the number of 2 address instructions are 3, calculate the possible combinations of one & zero address instructions. (10)
- 4) (a) Design a combinational circuit with 3 inputs & one output. The output is "1" when the input binary value is less than 3 & is "0" otherwise. (5 marks) (10)
(b) Design a combinational circuit for the following specifications: $Y = 1$, if A is 1 or B and C are 1. $Z = 1$, if B or C is 1 but not both or A, B, C are all 1. (5 marks)
- 5) Write the block diagram of a typical CPU model & explain the function of the following: (10)
 - a. General purpose registers
 - b. Dedicated registers
 - c. Control Unit

d. ALU

e. Dedicated hardware or firmware (2 X 5) marks

- 6) Design a 4 bit two input Adder & Subtractor unit using only 4 bit parallel adder unit. (10)
- 7) Write the internal architecture of 4X4 array multiplier and explain it's working (10)
- 8) Explain the effect of Cache memory with respect to speed of operation with a suitable diagram and an example. (10)
- 9) Assume cache has 3 blocks and initially all blocks are empty. Consider the following stream of block references 1,2,3,4,5,1,2,3,1,2,3,4,3,6,5
Calculate the hit ratio if the replacement policy used is (10)
(a) FIFO. (b) LRU. (c) Optimal replacement policy. (3+3+4) marks
- 10) (a) Explain the address translation using TLB. What are the advantages and disadvantages of this scheme? (10)
(b) The following measurements are obtained from a computer system with a TLB
- time taken to conduct a search in the TLB = 160 nsec.
 - main memory access time = $1\mu\text{sec}$.
 - Determine the average access time assuming a TLB hit ratio of 80%.



Copyright @ 2017 Littlemore Innovation Labs Pvt Ltd. IP: 52.66.163.73 epCloud 1.5
All rights reserved.