Question Paper

MANIPAL UNIVERSITY

SCHOOL OF INFORMATION SCIENCES (SOIS)
FIRST SEMESTER MASTER OF ENGINEERING - ME (VLSI DESIGN)
DEGREE EXAMINATION - APRIL 2017
Saturday, 22,2017
Time :10:00AM- 1:00PM

Digital Systems and VLSI Design [EDA 613]

Marks: 100 **Duration: 180 mins.**

Answer all the questions.

1)	Explain CZ method of crystal growth with relevant figures	(10)
2)	Explain P-well process with neat diagrams	(10)
3)	Explain, with a neat diagram, horizontal tube furnace system and its various sections used in thermal oxidation method	(10)
4)	What are the different ways of photoresist dispensing?	(10)
5)	What are the important second order effects in MOSFETs? Explain them briefly	(10)
6)	Derive an expression for the switching power dissipation component in a CMOS circuit. Discuss methods to reduce this component by analyzing each element in this expression	(10)
7)	Deduce the analytic delay models for the: (4 + 4 + 2) A) Fall Time B) Rise Time C) Delay Time	(10)
8)	Design a fully complimentary single bit full adder using minimum number of transistors. Using this adder, explain how do you construct an adder/subtractor circuit?	(10)
9)	Design a CMOS circuit for the Boolean expression F = ((A.B + C) D.E)' with equal rise time (t_r) and fall time (t_f).	(10)
10)		(10)

Design a CMOS inverter for which the inverter threshold is half the VDD and have equal rise time (t_r) and fall time (t_f).