MANIPAL UNIVERSITY

Question Paper

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MANIPAL UNIVERSITY

SCHOOL OF INFORMATION SCIENCES (SOIS)
FIRST SEMESTER MASTER OF ENGINEERING - ME (VLSI Design)
DEGREE EXAMINATION - APRIL / MAY 2017
Monday, 24,2017
Time :10:00AM- 1:00PM

High Level Digital Design [EDA 611]

Marks: 100 **Duration: 180 mins.**

A

Answer all the questions.

1)	What is VLSI design flow? Explain with a flowchart.	(10)
2)	Solve the logic equation $F(a,b,c,d)=\sum(0, 1, 5, 7, 8, 10, 14, 15)$	(10)
3)	Design a Moore machine with an example	(10)
4)	Explain Static Timing Analysis (STA) with necessary diagram & equations	(10)
5)	What is setup & hold time? How setup and hold violation can be fixed in a digital system, explain with an example	(10)
6)	What is false path in STA and how they impact the digital design	(10)
7)	Design synchronous FIFO using dual port memory	(10)
8)	Explain the Configurable Logic Block (CLB) with neat diagram	(10)
9)	Explain features of AMBA AHB bus and its components	(10)
10)	What is the Burst & Wrap Operation in AMBA bus explain with necessary timing diagram	(10)