Question Paper

MANIPAL UNIVERSITY

SCHOOL OF INFORMATION SCIENCES (SOIS)
FIRST SEMESTER MASTER OF ENGINEERING - ME (VLSI DESIGN)
DEGREE EXAMINATION - APRIL 2017
Friday, 28,2017
Time :10:00AM- 1:00PM

System on Chip Design [EDA 615.5]

Marks: 100 **Duration: 180 mins.**

Answer all the questions.

1)	Explain the array processor and vector processor models with the help of neat diagrams	(10)
2)	Mention the steps involved in the Electronic System Level flow. Explain the specification and modelling step with the help of examples	(10)
3)	List the four design principles in System on Chip architecture. Explain heterogeneous and distributed data storage principle	(10)
4)	Explain the processor core selection with the help of a flow chart	(10)
5)	What are the types of branch prediction? Explain bimodal and two level adaptive predictions	(10)
6)	How can we manage the out of order execution using sequential state register files?	(10)
7)	Explain set associative and direct mapping in cache organization with neat diagrams	(10)
8)	What is a Transaction Lookaside Buffer? How do we convert virtual addresses to real addresses?	(10)
9)	Draw and explain the a Core Connect-based System on Chip along with the transfer protocol using the processor local bus	(10)
10)	Describe static and dynamic networks in	(10)

Network on Chip.