Question Paper

MANIPAL UNIVERSITY

SCHOOL OF INFORMATION SCIENCES (SOIS)
FIRST SEMESTER MASTER OF ENGINEERING - ME (VLSI - DESIGN)
DEGREE EXAMINATION - APRIL 2017
Wednesday, 26,2017
Time :10:00AM- 1:00PM

Verification [EDA 617]

Marks: 100 **Duration: 180 mins.**

Answer all the questions.

1)	Discuss why verification is methodology based and not tool based.	(10)
2)	Describe the following with neat diagram. a. RTL Analysis (5) b. Equivalency checking (5)	(10)
3)	Explain about different types of Verification technologies	(10)
4)	Illustrate the following elements of Verification plan a. Models (5) b. Coverage Metrics (5)	(10)
5)	Differentiate Linear, random and self checking testbenches	(10)
6)	Explain the functionality of following verification environment components a. Transactor (Agent) (5) b. Scoreboard (5)	(10)
7)	Explain following code coverage's with examples. a. Finite State Machine Coverage (5) b. Expression Coverage (5)	(10)
8)	Explain about Covergroups in SystemVerilog with example	(10)
9)	Describe following with example a. Encapsulation (5)	(10)

b. Abstraction (5)

10) Explain the structure of assertions with an example (10)