MANIPAL UNIVERSITY

SCHOOL OF INFORMATION SCIENCES
SECOND SEMESTER MASTER OF ENGINEERING - ME (VLSI DESIGN)
DEGREE MAKE-UP EXAMINATION- JULY 2017
Monday, July 10, 2017
Time: 10:00 to 13:00

Advanced VLSI Design [EDA 604]

Marks: 100 **Duration: 180 mins.**

A

Answer all the questions.

1) A) What are the different ways of fabricating CMOS Resistors? (10)
B) Discuss the resistor layout techniques and practical considerations in a CMOS process.

2) What are the different types of MOSFET parasitic capacitances that show up at high frequency? Explain with a model. (10)

3) A) List the applications of a current source/current mirror. (10)
B) Design four current sinks with values 20, 30, 50 and 70 μA. What is the minimum voltage across each current sink?
Assume V_{DD} = +5V, V_{SS} = 0V, L = 5μm, V_{GS} = 1.2V, V_{th} = 0.83V, λ = 0.06/V, K_n = 50μA/V^2.

4) Explain the working of a regulated cascode current mirror with a neat schematic and a small-signal model. (10)

5) A) With the help of a diagram, explain a CMOS Common-Source amplifier with current source load. (10)
B) Calculate the small-signal voltage gain, Av, for the circuit shown in Fig. 5. Assume that M1 is biased in saturation and I1 is an ideal current source.
[Data: K_n = 50μA/V^2, W = 10μm, L = 5μm, V_{GS} = 1.2V, V_{th} = 0.856V,

$r_o = 1.7M\Omega$]

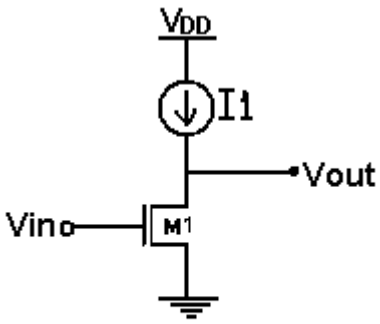

Fig. 5

6)	With a neat schematic diagrams, explain the Threshold Voltage Referenced Self-Biasing circuit	(10)
7)	With a neat schematic, derive an expression for small-signal voltage gain for an NMOS differential amplifier with passive resistor load	(10)
8)	What do you mean by charge injection and clock feedthrough in a MOSFET switch? Discuss a method used to reduce their effect.	(10)
9)	How an adaptive biasing circuit is better compared to an ordinary biasing circuit? With a neat schematic, explain an adaptively biased differential amplifier	(10)
10)	Derive expressions for $\|INL\|_{max}$ and $\|DNL\|_{max}$ for a simple Resistor string DAC	(10)