Question Paper

MANIPAL UNIVERSITY

SCHOOL OF INFORMATION SCIENCES (SOIS)
SECOND SEMESTER MASTER OF ENGINEERING - ME (VLSI DESIGN)
DEGREE EXAMINATION-APR / MAY 2017
Wednesday, 19, 2017
Time : 10:00 AM - 1:00 PM

Low Power VLSI Design [EDA 608]

Marks: 100 **Duration: 180 mins.**

Answer all the questions.

1)	List power dissipation components in digital CMOS circuits and explain	(10)
2)	How power can be reduced through Low power design through voltage scaling	(10)
3)	Explain the reliability driven voltage scaling. How they will affect different components in the transistor	(10)
4)	Design and explain Low to high level shifter	(10)
5)	List the rules to be followed for placing the level shifter in multi voltage domain	(10)
6)	List the principles of power gating design	(10)
7)	Explain the significance of header and footer fabric in power gating	(10)
8)	Design and explain the various retention register	(10)
9)	Design and draw the necessary waveform for the power control sequence without retention	(10)
10)	Discuss the dynamic voltage and frequency scaling	(10)