MANIPAL UNIVERSITY

Question Paper

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MANIPAL UNIVERSITY

SCHOOL OF INFORMATION SCIENCES (SOIS)
SECOND SEMESTER MASTER OF ENGINEERING - ME (VLSI DESIGN)
DEGREE EXAMINATION - APRIL 2017
Friday, 28, 2017
Time : 10:00 AM - 1:00 PM

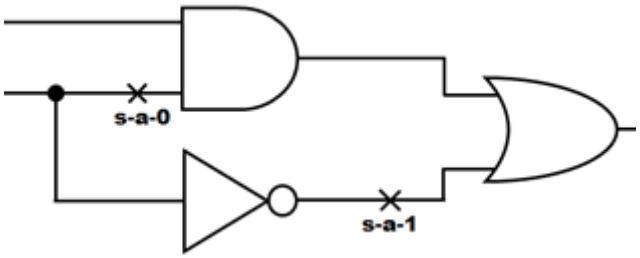
Physical Design [EDA 616.8]

Marks: 100 **Duration: 180 mins.**

A

Answer all the questions.

1)	State the static properties of Complementary CMOS Gates. Compare the Voltage Transfer Curves for of a two input NAND gate for different input combinations.	(10)
2)	What is Dynamic Logic in VLSI? Write a schematic of a four input NOR gate using Dynamic Logic.	(10)
3)	What is aspect ratio? Mention its effects in Floorplanning	(10)
4)	Explain Power Planning stage in Floorplanning of a VLSI chip	(10)
5)	Explain cluster and region in global placements	(10)
6)	What are the objectives of routing? Explain complete graph, Steiner minimal tree and half-perimeter methods in routing	(10)
7)	What are the advantages of modelling physical fault as a logical faults? Find out the collapse ratio for a two input XNOR gate built using NOR gates only.	(10)
8)	Explain stored pattern and pseudo exhaustive pattern generation	(10)
9)	Give the parallel vector pattern for finding the stuck at faults shown in the circuit.	(10)



10) Define Fault Model, Fault Coverage, Fault Simulation, Fault Equivalence, Fault Dominance in VLSI testing (10)