Question Paper

MANIPAL UNIVERSITY

SCHOOL OF INFORMATION SCIENCES (SOIS)
SECOND SEMESTER MASTER OF ENGINEERING - ME (VLSI DESIGN)
DEGREE EXAMINATION - APRIL 2017
Friday, 21, 2017
Time : 10:00 AM - 1:00 PM

Universal Verification Methodology [EDA 610]

Marks: 100 **Duration: 180 mins.**

Answer all the questions.

1)	Explain the functionality of following components with example. (5 + 5 =10 marks) a. Monitor b. Scenario Generator	(10)
2)	Explain Arrays in SystemVerilog.	(10)
3)	Explain the functionality of following with example (5 + 5 = 10 marks) a. Encapsulation b. Polymorphism	(10)
4)	Explain the functionality of following with example (5 + 5 = 10 marks) a. uvm_object class b. uvm_component class	(10)
5)	Explain the functionality of following (5 + 5 = 10 marks) a. Block level environment b. Integration level environment	(10)
6)	Explain different components in UVM Testbench.	(10)
7)	Illustrate UVM Factory coding convention 2 and convention 3 with example.	(10)
8)	Explain about UVM factory overrides.	(10)
9)	Write a note on creation of transaction using uvm_sequence with an example.	(10)

10) Explain the functionality of uvm_driver with example. (10)