Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

VI SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING) MAKE UP EXAMINATIONS, JUNE 2017

SUBJECT: EMBEDDED SYSTEM DESIGN [ELE4001]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 20 JUNE 2017** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.
- Support all your programs with relevant comments

1A. Classify embedded systems based on complexity and describe them in brief. Give relevant examples. ***(03)***

1B. Write a note on base line, mid-range and high performance '8' bit PIC microcontrollers. Give relevant examples. ***(03)***

1C. Explain the following with respect to assessing processor and computer performance.

i. Dhrystone benchmark.
ii. Other commonly used benchmarks for general purpose system.
iii. EEMBC for embedded systems. ***(04)***

2A. Describe the following ARM7 instructions. Illustrate with an example.

i. LDMIA R0, { R6, R2- R4}
ii. STMDA R10!, { R7 –R9} ***(03)***

2B. i. With the help of a relevant example, explain how pipe line flow in the execution of instructions improves the processor performance in case of ARM7TDMI.
ii. Illustrate with an example, how the pipe line flow is disturbed while executing LDR or STR instruction. ***(04)***

2C. Write an ARM7TDMI subroutine in assembly language to determine the binary equivalent of the ASCII code (for any hex number between '0' and 'F') passed to subroutine through R0 register; return the result through R1 and R2 registers. ***(03)***

3A. i. Describe the sequence of operation in ARM7TDMI when an exception occurs.
ii. Write a note on ARM7TDMI exception priority and nested exceptions.. ***(04)***

3B. Show the connection diagram to connect two push button switches to **p5 and p6**pins of mbednxplpc1768 microcontroller. Also connect a common anode type of 7 segment LED display to pins **p10 t0 p17**. Write a main program in 'C' to configure p5 and p6 as interrupt pins and keep waiting for an interrupt. When rising edge is detected at p5, write an ISR to display numbers '0' to '4' on the 7 segment display with a delay of 2.3 second and then return back; When falling edge is detected at p6, write an ISR to display numbers '9' to '5' on the 7 segment display with a delay of 1.9 second and then return back ***(03)***

3C. Describe and compare SRAM and DRAM memory devices. Write a brief note on DDRSDRAM ***(03)***

4A. Answer the following with respect to cache memory.

i. Memory hierarchy in a system with two levels of cache and main memory. Describe the method used by processor to access memory (read operation) in such a system.

ii. Describe the various cache replacement techniques along with their relative merits and demerits. ***(04)***

4B. With the help of a relevant timing diagram, describe the PCI parallel communication protocol for memory write operation to transfer three '16' bit data. Assume that no extra cycle is required during first data, two extra cycles requested by initiator for second data and one extra cycle requested by target in case of third data. ***(03)***

4C. i. List the salient features and specifications of CAN serial communication bus.

ii. Bus arbitration scheme used (describe CSMA / CD protocol). ***(03)***

5A. Write a 'C' program for PIC16f877 microcontroller to configure the MSSP in SPI master mode to transmit data bytes 28H and 4AH to a slave device connected to RB6 pin at a baud rate of 1.25Mbps and store the received data bytes. Idle state for clock is low level, transmit data on the falling edge, and sample input data at the middle of data output time. Assume fosc = 20MHZ. ***(04)***

5B. Write a 'C' program to convert the analog input applied to RE1 / AN6 pin of PIC16f877 microcontroller and display the result at ports 'C' and 'D'. Use right justified result, conversion time of 24μs, positive and negative reference voltages from RA3 / AN3 and RA2 / AN2 pins. All the remaining pins of ports A and E should be available as analog input pins. Take F_{osc} = 4MHz. ***(03)***

5C. Three peripherals '1', '2' and '3' are to be connected to a processor in daisy chain arbitration scheme. Peripheral '1' is closest to processor. However peripherals 2 and 3 are daisy chain compatible, whereas peripheral 1 is not daisy chain aware. Design a suitable logic circuit to make peripheral 1, daisy chain compatible. Describe the daisy chain operation in this system, considering a relevant example. ***(03)***