Reg. No.



## VI SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING) END SEMESTER EXAMINATIONS, APRIL - MAY 2017

## SUBJECT: EMBEDDED SYSTEM DESIGN [ELE4001]

REVISED CREDIT SYSTEM

Time:	: 3 Hours	Date: 27, April 2017	Max. Marks: 50
Instru	<ul> <li>Answer ALL the questions.</li> <li>Missing data may be suitably</li> <li>Support all your programs w</li> </ul>	•	
1A.	Describe the method of increasing	o increase the processing power of a proces ng the processing power using multiproces ite a brief note on 8087 NDP (numeric data	sor (main and co-
1B.	Describe the following instruction I. CLRF f II. IORWF f,d III. SUBLW K IV. BTFSS f,b	ons of PIC16f877 microcontroller. Illustrate	with an example. (04)
1C.	Show the connection diagram to connect two push button switches to RC6 and RC7 pins and red and green LEDs to RB3 and RB4 pins of PIC16f877microcontroller. Also show the power supply, reset and system clock connections. Write an assembly code to turn on the red LED when switch connected to RC6 is closed and turn it off after a suitable delay. Similarly, turn on the green LED when switch connected to RC7 is closed and turn it off after a suitable delay. When no switch is closed, keep both the LEDs in off position.		
2A.	<pre>i. Write ARM7 assembly co variables 'a' to 'g' respect if ( a = = b    c = = d) {</pre>	ode for the following 'C' code. Consider regi tively.	sters R0 to R6 for
	ii. Write single ARM7TDMI	I instruction to clear MS bit (bit D31) of R( r if the negative flag is set.	) register without <b>(03)</b>
2B.		g of various types of stack with respections of ARM7TDMI to implement these states and the states and the states are states as a state of the states are states as a states are states as a state of the states are states as a state of the states are states as a states are states as a states are states as a state of the states are states as a state of the states are states as a state of the states are states are states are states as a state of the states are states are states as a state of the states are states as a state of the states are states as a state of the states are states as a states are states are states as a state of the states are states as a state of the states are st	t to ARM7TDMI
<b>2C</b> .	of two non-zero positive numb	e in assembly language to determine the GC pers passed to the subroutine through reg	

Return the result through R2 (GCD) and R3 (LCM).

- **3A.** i. Describe the data abort exception of ARM7TDMI processor (When does this exception occur? What is expected to be done in data abort exception handler and instruction used to return from this exception).
  - ii. Assuming that you are writing code for reset exception, write ARM7TDMI instructions to enable IRQ and FIQ interrupts and change the mode of operation to user mode.
- **3B.** Show the connection diagram to connect two push button switches to **p10 and p11** pins of mbednxplpc1768 microcontroller. Also connect a common anode type of 7 segment LED display to pins **p20 t0 p27**. Write a main program in 'C' to configure p10 and p11 as interrupt pins and keep waiting for an interrupt. When rising edge is detected at p10, write an ISR to display numbers '0' to '5' on the 7 segment display with a delay of 3.2 second and then return back; When rising edge is detected at p11, write an ISR to obtain 100 cycles of 100Hz., 35% duty cycle rectangular waveform at the CRO connected to **p28** pin and then return back.
- **3C.** Describe and compare EPROM and EEPROM memory devices.
- **4A.** i. Describe the developments and current trends with respect to cache memory.
  - ii. In a system with two levels of cache, out of 1300 memory references, there are 90 misses in L1 cache and out of that 40 misses in L2 cache. L1 access time is 2 clock cycles, L2 access time is 11 clock cycles and main memory access time is 95 clock cycles, determine the average memory access time. What will be the average access time if L2 cache is not included in the system (only L1 cache present).
- **4B.** Describe the bus arbitration scheme used by PCI parallel communication bus to support multi master configuration.

Explain the functions of following signals (pins) of PCI bus

i. C/BE 3 – C/BE 0 ii. FRAME iii. DEVSEL

- **4C.** i. With the help of a relevant diagram, describe the connection of various devices to USB (using tiered star topology).
  - ii. List the various data transfer rates supported by USB.
- **5A.** Write a 'C' program for PIC16f877 microcontroller to configure the MSSP in I2C master mode to transmit data bytes 5AH, 6BH and 7CH to a slave device with address 2DH at a baud rate of 400kbps. Assume fosc = 16MHZ.
- **5B.** Answer the following with respect to on chip ADC of PIC16f877 microcontroller.
  - i. Determine the values of ADRESH and ADRESL registers , with left justified result format, when the analog input applied is '3.8' V, positive reference voltage is '4.5' V and negative reference voltage is '0' V
  - ii. Determine the values to be loaded to ADCON0 and ADCON1 registers values for the following configuration: Turn on ADC,  $F_{ADC}$  (clock) derived from internal RC oscillator, select RA0/ AN0 input channel, right justified result, positive and negative reference voltages from  $V_{DD}$  and  $V_{SS}$  pins, only RA0 is analog input and remaining pins of ports A and E should be digital I / O pins.
- 5C. With the help of a relevant diagram, describe the Priority arbitration scheme for expanding the number of interrupts to a processor. List the merits and demerits of this scheme by comparing it with daisy chain arbitration scheme. (03)

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