Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

SIXTH SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION - APRIL / MAY 2017
SUBJECT: ASIC (ECE - 320)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ANY FIVE** full questions.
- Graph sheets will be provided
- Missing data may be suitably assumed.

1A. Implement 0101 sequence detector using PLA and D flip flop

1B. Explain the working of SRAM cells

(6+4)

2A. Perform the KL algorithm on the circuit shown in the **FIGURE Q2A** using {423,156} as initial partition.

2B. What is Placement? What is the importance of placement?

(6+4)

3A. Given netlist with five blocks a-e, starting block a, and six nets N1-N6. N1 = (a,b), N2 = (a,d), N3 = (a,c,e), N4 = (b,d), N5 = (c,d,e) and N6 = (d,e). Find a linear ordering using the linear ordering algorithm.

3B. What is floor planning and why it is important?

(6+4)

4A. Show that the diffusion capacitance of conventional 24/12ʎ CMOS inverter is reduced by 50% after the layout folding. Draw the folded layout. Given that a unit transistor with width =4ʎ offers the diffusion capacitance C.

4B. What is supply bounce? Explain with an example.

(6+4)

5A. Implement a 3 bit ring counter using Xilinx XC 3000 FPGA. Show the proper routing and specify the number of CLB's and LUTs required to implement the design

5B. Find the propagation and contamination delay for the circuit shown in **FIGURE Q5B**

(6+4)

6A. Perform Stockmeyer algorithm on the slicing floorplan that is represented by 435H1V 67VH2V 8HV. The dimension of the modules 1 through 8 are *{*(5,3), (2,3), (6,3), (2,5), (6,2), (5,1), (3,8), (6,3)*}*. Draw the floorplans before and after the orientation optimization.

6B. Calculate the maximum operating frequency for the circuit shown in **FIGURE Q6B**

(6+4)

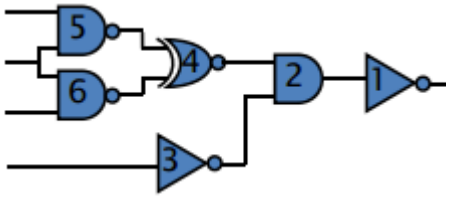

FIGURE Q2A

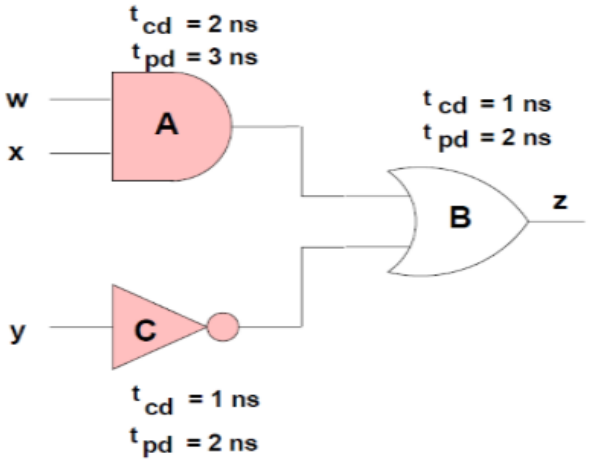

FIGURE Q5B

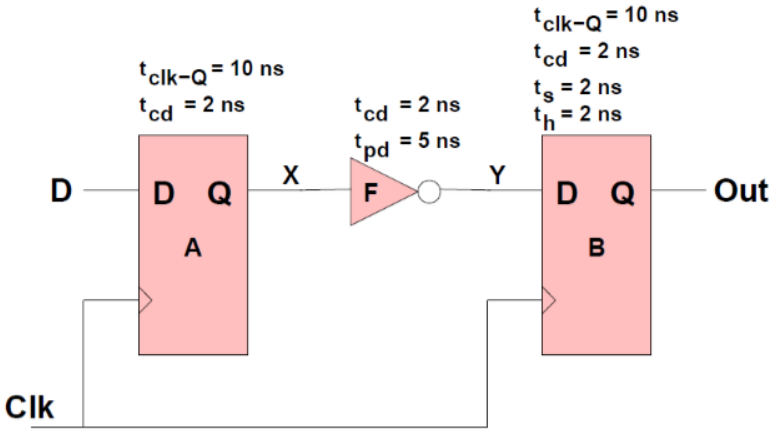

FIGURE Q6B