Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

SIXTH SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION - April/May 2017

SUBJECT: EMBEDDED SYSTEM DESIGN (ECE - 4003)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Assume that inputs 'X' and 'Y' are available from memory. The single purpose processor is intended to perform X ÷ Y through repeated subtraction. The calculated quotient is saved back in the memory. Assume X>Y, Y≠ 0 and X=Y=4 bits. Design and draw the datapath of the processor with control signals been indicated.

1B. Write two valid differences between the types of processor technologies.

1C. The availability of an embedded product is 90%. The MTBF of the product is 30 days. What is the MTTR in days of the product?

(5+3+2)

2A. Write the significance of the following:
(a) PPI (b) Reset circuit (c) RTC (d) Memory shadowing (e) Oscillator unit

2B. Explain the different types of data transfers supported by USB.

2C. Explain the following addressing modes used in General purpose processor with an example for each.
(a) Direct addressing mode (b) Register indirect addressing mode

(5+3+2)

3A. Differentiate between the following:
(a) SRAM and DRAM
(b) Processor architectures.
(c) Bluetooth and Zigbee
(d) 8051 power management modes.
(e) GPRS and Wi-Fi

3B. What is EDLC? What are its objectives?

3C. List the different power reduction techniques used in designing low power embedded systems.

(5+3+2)

4A. Consider a case where process ID's P1, P2, P3 with estimated completion time 10, 8, 3 milliseconds is supposed to enter the ready queue together in the order P2, P3, P1. Process P4 with estimated execution completion time 4 milliseconds will enter the ready queue after 8 milliseconds. Which scheduling algorithm (LIFO or FIFO) is suitable for the given case?

4B. Explain the following:
(a) Multithreading (b) Remote procedure call (c) Livelock

4C. With a neat diagram explain Process life cycle.

(5+3+2)

5A. What is scheduling and binding? For the given function below draw the following:

$$F = (a \times b) + (c \times d) + (e \times f) + (g \times h)$$

i) The data flow graph.

ii) The scheduling and binding of the code.

iii)The final data path.

iv)The controller.

Note: Use 2:1 MUXs, single adder and two multipliers in the final data-path.

5B. A door sensor is connected to P1.1 pin, a buzzer is connected to P1.7 pin and a Common cathode 7-segment display to port 2 of the 8051 controller. Write an embedded C program to continuously monitor the door sensor, turn ON the buzzer and display "O" in the 7-segment display whenever the door opens. When the door is closed display "C" in the 7-segment display.

5C. Explain the following:

(a) Cross compilers (b) Emulators

(5+3+2)