Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
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SIXTH SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION - APRIL / MAY 2017

SUBJECT: EMBEDDED SYSTEM DESIGN (ECE - 4003)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Assume that inputs 'A' and 'B' are available from memory. The single purpose processor is intended to perform A x B through repeated addition. The calculated product is saved back in the memory. Assume X=Y=4 bits. Design and draw the datapath of the processor with control signals been indicated.

1B. Write two valid differences between the types of IC technologies.

1C. Define time to prototype. The time to prototype a commercial embedded product was 2months and time to market was 2 years. What is the turn-around time of the product?

(5+3+2)

2A. Write the significance of the following:
(a) PPI (b) Brown out protection circuit (c) RTC
(d) Memory shadowing (e) IDE

2B. With a neat diagram, explain data transfer in SPI interface.

2C. Identify the following addressing modes used in General purpose processor.
(a) MOV R0, 1000h (b) MOV R3, @R0

(5+3+2)

3A. Differentiate between the following:
(a) SRAM and DRAM
(b) General purpose Timer and watch dog timer.
(c) Endianness in processor/controller
(d) 8051 power management modes.
(e) Bluetooth and Zigbee

3B. What is EDLC? What are its objectives?

3C. Consider an embedded system with three different voltage levels. Energy consumption per cycle is

shown in the TABLE Q3C. If a task T with 10^9 cycles needs to meet a deadline of 20 seconds, which of the three voltage levels will minimize power consumption?

TABLE Q3C

V_{dd} (V)	5	4	3
Energy per cycle (mJ)	40	25	10
Frequency (MHz)	50	40	25

(5+3+2)

4A. Processes with process IDs P1, P2 and P3 with estimated completion time 8, 4, 7 milliseconds respectively enter the ready queue together in the order P3, P2 and P1. Process P4 with estimated completion time 4ms enters the ready queue after 2ms. Process P2 enters the Blocked state after 2ms of starting of its execution and has an IO waiting time of 3ms. All the estimated execution completion time is excluding I/O waiting time. Which scheduling algorithm (LIFO or FIFO) is suitable for the given case?

4B. Explain the following:

(a) Deadlock (b) Remote procedure call (c) Binary semaphore

4C. Differentiate between:

(a) Types of kernels (b) Types of OS

(5+3+2)

5A. LEDS are connected to Port 1 and port2 of 8051 MC. Write an embedded C program to continuously receive bytes serially at 9600 baud, check the bytes if they are even or odd. If they are even then display them in Port1. If they are odd then display them in port 2. Use a function to receive bytes serially.

5B. Design a data path and controller for the following function. Show all the steps.

$$\boldsymbol{F = (a + b) \times (c - d) \times (e + f) \times (g - h)}$$

Note: Use 2:1 MUXs, single adder, subtractor and multiplier in the final data path.

5C. Identify and draw the computational models involved in question 5A.

(5+3+2)