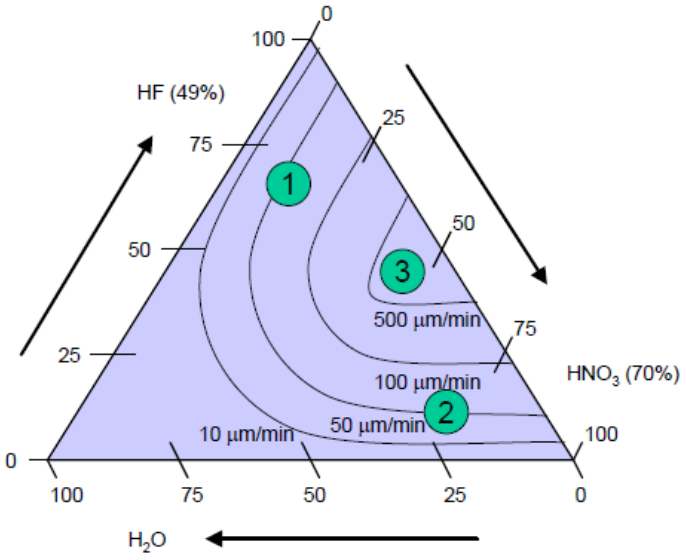
Reg. No.										

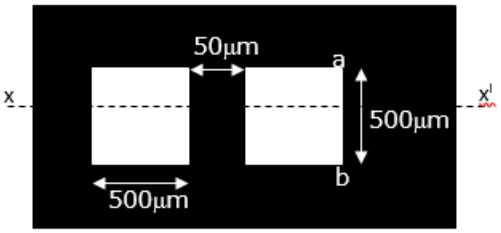
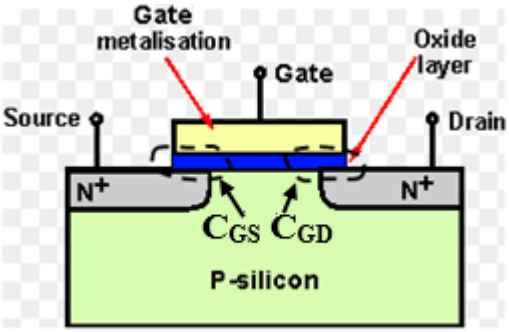
MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

VI SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION - April/May 2017
SUBJECT: VLSI/ULSI PROCESS TECHNOLOGY (ECE - 4016)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A.	Define linear density. Derive the expression for the same for a BCC [110] directions in terms of the atomic radius R. Define planar density. Derive planar density expression for a FCC (100) planes in terms of the atomic radius R. Define packing density. Obtain the packing density value for a simple cubic lattice
1B.	Explain FZ technique of growing single crystal silicon. What are its merits and demerits? What property of material is exploited in this technique?
1C.	In the isoetch contours shown in Fig. 1(C), write the features of region 1, 2 and 3.  **Figure 1(C)** (5+3+2)
2A.	(i) For an oxidation process B=0.287 µm^2/hr, A=0.226 µm and τ=0. Determine till what oxidation time the oxidation rate may be approximated to be linear. (For this approximation, the error between exact and linear approximation values should be within 10%. (ii) What is the effect of boron on oxidation rate? (iii) What is the effect of crystal orientation on oxidation rate? (iv) If we perform an oxidation process with dry for some time followed by wet for some time, what care should be taken in calculating the total oxide thickness. Explain. (v) If the oxidation is performed at same temperature, but at an elevated pressure, comment on the thickness of the grown oxide.
2B.	Write on molecular beam implantation. When are they used in place Ion implantation?
2C.	List the merits and demerits of dry etching over wet etching. (5+3+2)
3A.	(i) A pre-deposition of boron is carried out for 15 minutes on an n-type silicon wafer with a bulk doping concentration of 10^{17} atoms/cm^3 at 950^{o}C. Determine the p-n junction depth given that the

	solid solubility of boron at 950°C is 3.8×10^{20} atoms/cm^3, the intrinsic diffusivity (D_0) is 0.76cm^2/s, and the Arrhenius activation energy (E_A) is 3.46 eV. (ii) A drive-in process is subsequently performed to produce a p-n junction at a depth of 1.28µm. Estimate the required Dt. Based on your result, determine the time required if the drive-in temperature is 1250°C. Given: $D=D_0\exp(-E_A/kT)$, $D_0=10.5$cm^2/sec, $E_A=3.69$eV, Boltzmann Constant$=1.38\times10^{-23}$J/K$=8.617\times10^{-5}$eV/K
3B.	With necessary diagrams, explain the lift off technique. What are the uses of such technique? What is the precaution to be taken in successfully achieving the lift off process?
3C.	What are the main features of X-ray, e-beam, and ion beam lithography? Explain. (5+3+2)
4A.	On a 300µm thick (100) silicon wafer, etching is carried out using the mask pattern of Fig. 4(A) with side 'ab' aligned along <110> primary cut. If the etch depth is 100µm, draw the cross-section along x-x^I if the etching is carried out using i) KOH – anisotropic etching with 111 plane acting as etch stop ii) HNA – isotropic etchant iii) RIE – anisotropic and plane independent  **Figure 4A**
4B.	Explain the various ways of realizing capacitors in an IC.
4C.	What are the possible ion stopping mechanisms in an Ion implantation system? Explain. (5+3+2)
5A.	Figure 5A is a p-channel MOSFET structure. The separation between two N^+ regions is 5µm, Gate metal area is 6µm×6µm, and oxide layer thickness is 100nm. Calculate Gate to Source (C_{GS}) and Gate to Drain (C_{GD}) overlap capacitance. (i) Gate metal is perfectly aligned (ii) Gate metal is shifted to right by 0.5µm (iii) Gate metal is shifted to right by 1µm (iv) Repeat part (i) to (iii) if Gate metal area is increased to 7µm×7µm. (v) In step (iv), by what percentage capacitance changes in respective cases?  **Figure 5A**
5B.	With necessary diagrmas, explain the various types of diffusion mechnisms.
5C.	What is self-aligned process? Explain with necessary diagrams. Why is it popular? explain (5+3+2)