Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
Manipal University

SIXTH SEMESTER B.TECH (E & C) DEGREE END SEMESTER EXAMINATION - APRIL / MAY 2017

SUBJECT: VLSI/ULSI PROCESS TECHNOLOGY (ECE - 4016)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions. Missing data may be suitably assumed.

1A. With respect to the data given for the two CZ processes, answer the questions given.

	CZ Process 1	CZ Process 2	Question
Dopant	Arsenic	Boron	***
Segregation Coefficient	0.3	0.8	***
Initial Dopant Concentration (cm^{-3})	10^{17}	?	Determine the initial concentration in process 2, such that seed end has concentration same as the one obtained in Process1
Initial Dopant Concentration (cm^{-3})	10^{17}	10^{17}	For both processes, till what percentage of melt is solidified, the dopant concentration is within 10% initial concentration?
Initial Dopant Concentration (cm^{-3})	10^{18}	10^{17}	What percentage of melt should be solidified in process 2 to get the concentration same as that the concentration obtained in process 1 when 30% of melt is solidified?
Initial Dopant Concentration (cm^{-3})	10^{17}	10^{17}	For the two cases, what is the ratio of concentration when 90% melt is solidified to 10% melt is solidified?
Initial Dopant Concentration (cm^{-3})	10^{17}	10^{17}	What is the percentage of melt solidified in process 2 if the ratio of concentration when 90% melt is solidified to 10% melt is solidified is identical for the two cases?

1B. What are epitaxial systems? Explain.

1C. What does (h k l), <h k l>, [h k l], {h k l} represent? Sketch each one of them in a unit cell.

(5+3+2)

2A. A <100> silicon wafer has a 2000Å oxide on its surface

(i) How long did it take to grow this oxide at 1100°C with dry oxidation?

(ii)The wafer is put back in the furnace for wet oxidation at 1000°C. How long will it take to grow an additional 3000 Å of oxide?

(iii) A <111> type wafer is dry oxidized for the time and temperature of part(i), will the grown oxide thickness be more than 2000Å or less? Why? Explain. Boltzmann Constant=1.38×10^{-23}J/K=8.617×10^{-5}eV/K

	Dry	Wet
$B=C_1\exp(-E_1/kT)$	$C_1=7.72\times10^2\mu m^2/hr$ $E_1=1.23eV$	$C_1=3.86\times10^2\mu m^2/hr$ $E_1=0.78eV$
$B/A=C_2\exp(-E_2/kT)$	$C_2=3.71\times10^6\mu m/hr$ $E_2=2.00eV$	$C_2=0.97\times10^8\mu m/hr$ $E_2=2.05eV$

2B. i) List the merits and demerits of Ion implantation over diffusion.
ii) What is channelling effect in Ion implantation? What are the techniques to mitigate the same?

2C. Sketch within a cubic unit cell the following planes (i) (2 -1 2) (ii) (2 1 0).

(5+3+2)

3A. In a two-step process, phosphorus was diffused into a p-type silicon wafer ($N_B = 10^{16}$ cm^{-3}). In the deposition step, the temperature was 900°C and the diffusion time was 45 minutes. In the drive-in step, the temperature was 1100°C and the time was 60 minutes. Calculate the surface concentration and Junction depth. Solid solubility of phosporous in silicon at 900°C is $7x10^{20}$ cm^{-3}, D_0=10.5cm^2/sec, E_A=3.69eV, Boltzmann Constant=1.38×10^{-23}J/K=8.617×10^{-5}eV/K.

3B. With necessary diagrams, explain the various p-n junction isolation techniques.

3C. What are high-k dielectrics? Why they are important? Explain.

(5+3+2)

4A. A square window of 500μm×500μm is opened on a silicon wafer with SiO_2 as mask layer. The window edges are aligned along 110 directions. Etch rate of silicon in KOH is 1μm/minute and that of SiO_2 is 2nm/minute. Neglect the etch rate of 111 plane.

i) What is the etch depth and etch pattern at the end of 20minute etching?
ii) At what depth and time the slow etching 111 planes merge?
iii) What is the etched volume at the end of step2?
iv) What is the oxide thickness required to complete the etch process of step 2?
v) What should be the window size on one side to get a through hole with a window size of 100μm×100μm on the other side?

4B. Explain the various ways of realizing resistors in an IC.

4C. What is 'Latch up' in CMOS devices? What are the possible solutions to overcome the same?

(5+3+2)

5A. Figure 5(a) to (e) represents the intensity of light falling on the PPR which is spun on a substrate material. For the PPR, $D_{100} \geq 2I$ and $D_0 < 2I$. Plot the pattern of the PPR on developing.

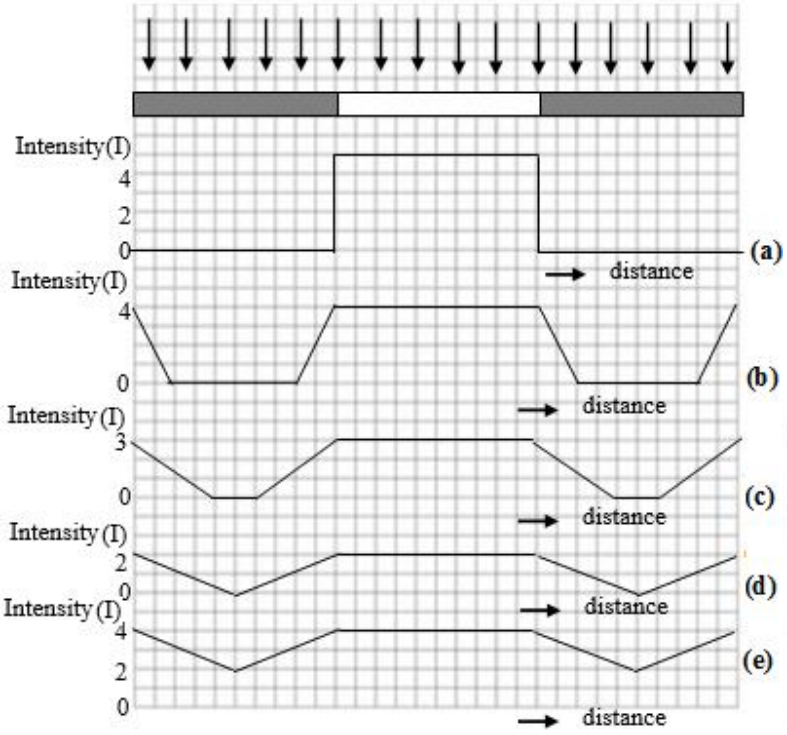

Figure 5

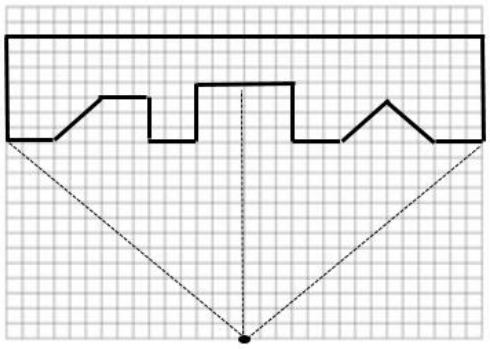

Figure 5(b)

5B. Figure 5(b) represents a thermal evaporation process with a point source. Is there any shadow region where no metal will be deposited? Determine the length of the wafer on which metal is deposited. Assume each cell size is 1×1mm.

5C. What is electromigration? Explain with necessary diagrams. (5+3+2)