Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

SIXTH SEMESTER B.TECH (INSTRUMENTATION & CONTROL ENGG.)

END SEMESTER EXAMINATIONS, JUNE 2017

SUBJECT: DIGITAL SYSTEM DESIGN [ICE 4001]

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A What are the differences between structural and behavioral style of VHDL coding? 2

1B Develop a state graph and transition table to detect an overlapping sequence 1101. Assume it to be a Moore Machine. 3

1C Write a behavioral VHDL code based on the state graph developed above. 5

2A Fix the following VHDL code 2

```
entity exam is
   port(a, b,: in bit;
        c          : out bit);
end examination;

architecture sequential of exam is
    process(a)
    begin
          c= a and b;
end exam;
```

2B If A = “110”, B = “111” C “011000” then evaluate the following 3

i. A & not B
ii. C ror 2
iii. A srl 2

2C Develop the circuit for a full adder using two half adders. Assuming components, with suitable interconnects, write a structural VHDL code for the same. 5

3A With a neat diagram for 4:1 mux, realize using when else statements. 2

3B Draw a neat Y chart showing the different levels of abstractions in the 3 domains. 3

3C What are s-a-0 and s-a-1 faults? How do they occur? What are their consequences on the circuit? How can they be tested? Explain with an example. 5

4A Write a VHDL code for a positive edge triggered T flip-flop. 2

4B Explain IF ELSE statements with an example. 3

4C What is propagation delay? What is its relationship with setup and hold time? 5

In the Fig Q4C, D flip-flop has a setup time of 4 ns, a hold time of 2 ns, and a propagation delay from the rising edge of the clock to the change in flip-flop output in the range of 6 to 12

ns. The XOR gate delay is in the range of 1 to 8 ns.

(i) What is the minimum clock period for proper operation of the following network?

(ii)What is the earliest time after the rising clock edge that X is allowed to change?

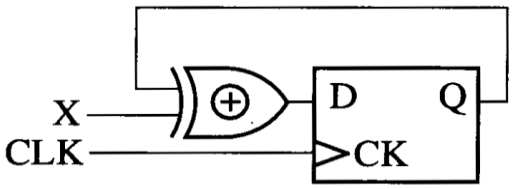

Fig Q4C

5A	What is a test bench? Where are they used?	2
5B	With neat diagrams, explain the various FPGA architectures.	3
5C	For the timing diagram shown in Fig Q5C, develop a VHDL code.	5

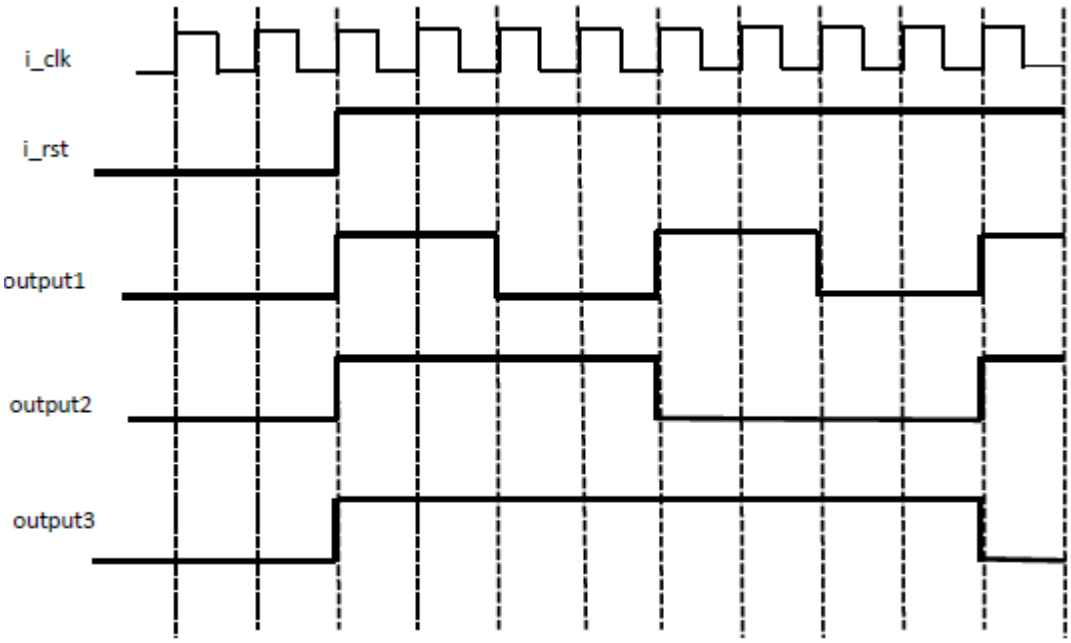

Fig Q5C

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