Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
A Constituent Institution of Manipal University

SIXTH SEMESTER B.TECH. (INSTRUMENTATION AND CONTROL ENGG.)

END SEMESTER EXAMINATIONS, APRIL/MAY 2017

SUBJECT: DIGITAL SYSTEM DESIGN [ICE 4001]

Duration: 3 Hour | Max. Marks:50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1	(a)	Show that i) $A+BC = (A + B)(A + C)$ ii) $A+B[AC + (B + \overline{C})D] = A + BD$	2
	(b)	Reduce using K Maps $F = \sum m(0,2,3,5,6,7,8,10,11) + \sum d(14,15)$	3
	(c)	For the input sequence X = 0011011001010100, design a Mealy circuit that generates the output Z = 0000010000010100. Draw the state graph, state table, transition table and output circuit.	5
2	(a)	Draw the block diagram for a Moore machine. What is the difference between a Mealy machine and a Moore machine.	2
	(b)	Draw a near Y chart showing the different levels of abstractions in the 3 domains.	3
	(c)	Design a full adder using two half adders. Develop a structural VHDL code for the same. Assume necessary components.	5
3	(a)	Write a VHDL code for a negative edge triggered D Flipflop with active high reset.	2
	(b)	Explain case statements using an example.	3
	(c)	Develop a state graph to detect the sequence 1000. Write a behavioral code for the same.	5
4	(a)	Explain path sensitization with two level AND OR circuit.	2
	(b)	With a neat timing diagram illustrate and define setup time and hold time.	3
	(c)	For a 25 MHz clock, with appropriate signal declarations write a VHDL code to generate a 'single cycle done' signal at the end of 200 µs. Draw a timing diagram for the same.	5
5	(a)	Realize the function $f(A,B,C) = \sum(0,1,2,4)$ using PLA.	2
	(b)	What are the types of operators in VHDL. Give an example for each.	3
	(c)	With neat diagrams, explain various FPGA programming technologies.	5