Reg. No.										

Manipal Institute of Technology, Manipal

(A Constituent Institute of Manipal University)

VI SEMESTER B.TECH (MECHATRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, JUNE/JULY 2017

SUBJECT: FPGA BASED DIGITAL SYSTEM DESIGN [MTE 4104]

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. A stepper motor drive circuit requires four signal waveforms given in **fig.Q1(A)** .Design a Mealy type sequence generator to provide the necessary signals for the stepper-motor drive using suitable ACTEL ACT 2, S and C logic modules **(5M)**

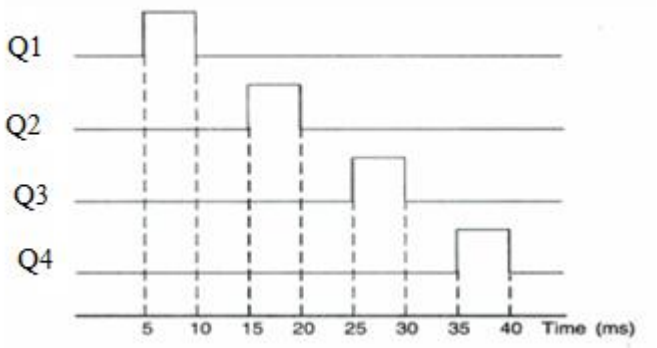

fig.Q1(A)

1B. Write a Verilog HDL code to design parallel adder cum subtractor using Full adder as sub module and Half adder as Leaf cell in gate level modeling. **(5M)**

2A. Find the faults that can be detected for the logic diagram shown in **fig.Q 2(A)** by test vector {11} using parallel fault simulation with a machine word length W=3. **(2M)**

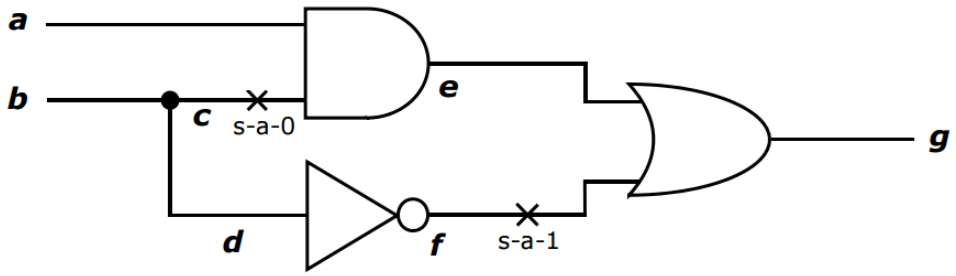

fig.Q 2(A)

2B. Write a Verilog HDL code to design a frequency divider that generates 25MhHz from 100MHz input. **(3M)**

2C. Design 3-bit Jhonson counter using ACTEL ACT-3 logic modules. **(5M)**

3A. Design 2-bit comparator using Xilinx 3000 series FPGA Logic block(s). **(4M)**

3B. Implement Binary to Excess3 Code converter using ROM. **(3M)**

3C. Write a Verilog HDL code to design BCD adder using dataflow modeling. **(3M)**

4A. Implement the following functions in PAL **(5M)**

$W(A,B,C,D) = \sum m(2,12,13);$
$X(A,B,C,D) = \sum m(7,8,9,10,11,12,13,14);$
$Y(A,B,C,D) = \sum m(0,2,3,4,5,6,7,8,10,11,15);$
$Z(A,B,C,D) = \sum m(1,2,8,12,13)$

4B. Write an ALU coding to perform addition, subtraction, multiplication and division operations using function as a single module and call this function to top module. **(5M)**

5A. Write a Verilog HDL code to design overlapping sequence detector 1011 using Mealy model. **(4M)**

5B. Find the test vector for the logic circuit shown in **fig.Q5(B)** using Path sensitization method (α is s-a-0) **(3M)**

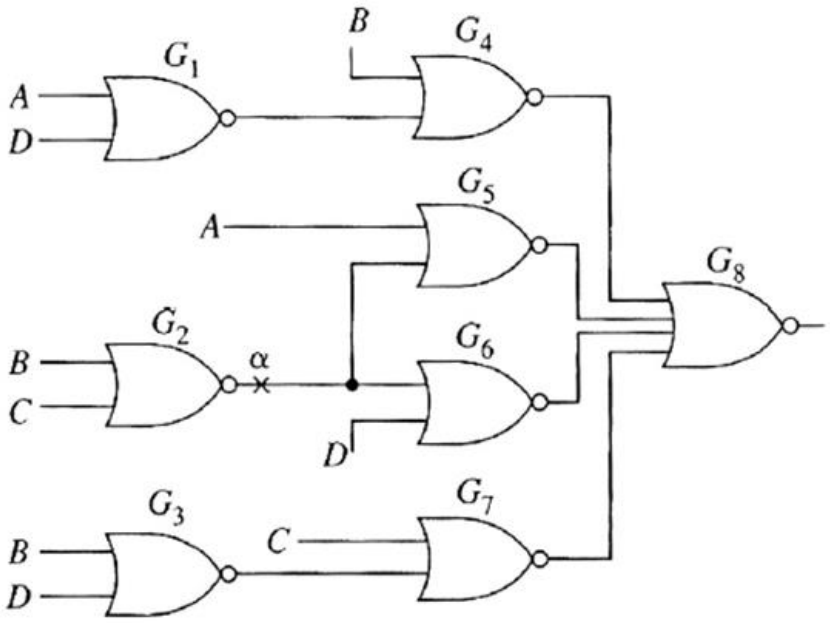

fig.Q5(B)

5C. Generate the signature for the logic circuit shown in **fig Q5(c)** **(3M)**

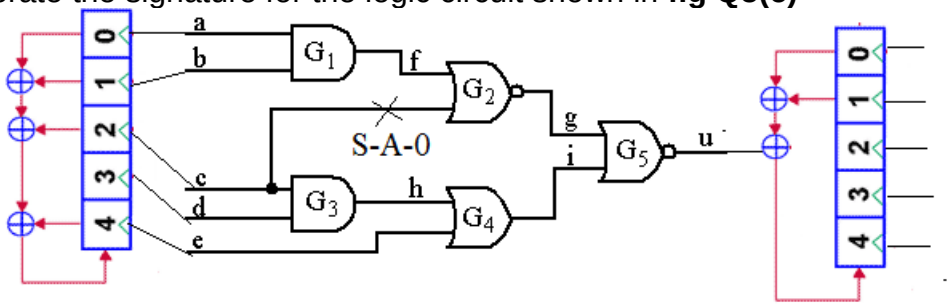

fig Q5(c)