Reg. No.										

Manipal Institute of Technology, Manipal

(A Constituent Institute of Manipal University)

VI SEMESTER B.TECH (MECHATRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, APRIL/MAY 2017

SUBJECT: FPGA BASED DIGITAL SYSTEM DESIGN [MTE 4104]

Time: 3 Hours **REVISED CREDIT SYSTEM** MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Implement the following functions in appropriate PLA **(3M)**

$$F_1 = A\bar{B} + AC + \bar{A}B\bar{C}\ ;\ F2 = \overline{(AC + BC)}$$

1B. Find the faults that can be detected for the logic diagram shown in **fig.Q 1(B)** by test vector 10010 using deductive fault simulation. **(2M)**

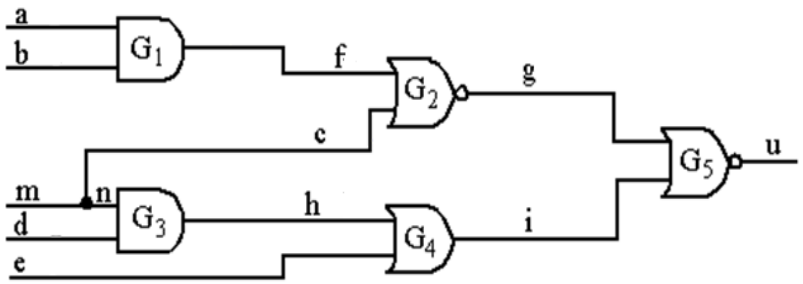


fig.Q 1(B)

1C. Write a Verilog HDL program to design Timer Based Single Way Traffic Light Controller using FSM Technique. **(5M)**

2A. Find the test vector for the logic circuit shown in **fig.Q 2(A)** using D-algorithm **(3M)**

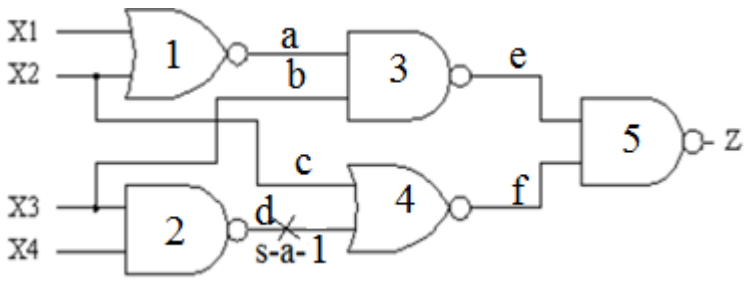


fig.Q 2(A)

2B. Write a Verilog HDL program to design 2-input CMOS OR gate using switch level modeling. **(3M)**

2C. Design 3-bit UP counter using ACTEL ACT- 3 logic modules **(4M)**

3A. Implement the function $f(x) = x^2$ in appropriate ROM (x is a 3-bit binary no.) **(3M)**

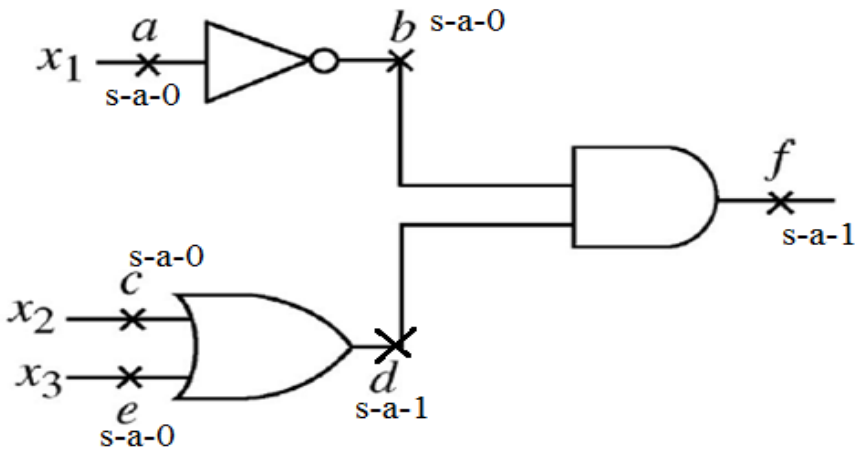
3B. Write a Verilog HDL program for detecting the number of 1's in an 8-bit vector using behavioral modeling. **(3M)**

3C. Write a Verilog code for overlapping sequence detector 1011 using Moore model **(4M)**

4A. Write a Verilog HDL program to detect falling edge of a signal using behavioral modeling. **(3M)**

4B. Create a user defined primitive (UDP) for a JK flipflop using "?" and "-" if needed. **(3M)**

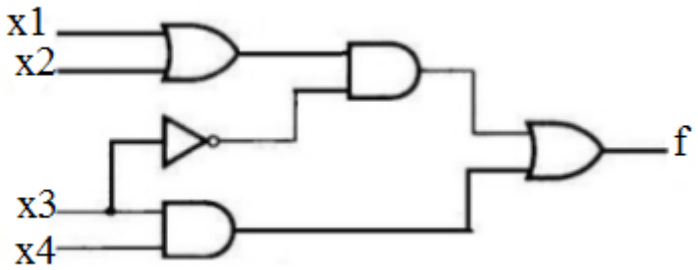
4C. Find (a) Fault matrix (b) minimal test set for the circuit under test (CUT) shown in **fig.Q 4(C)**



(4M)

fig.Q 4(C)

5A. For the circuit depicted in the **fig.Q 5(A)** use the Boolean difference method to find all the tests (that is, combination of input variable values) for X3 at s-a-0



(3M)

fig.Q 5(B)

5B. Write a Verilog HDL program to design 1024x16 RAM using behavioral modeling. **(3M)**

5C. Design 0101 sequence detector(overlapping allowed) using XILINX XC3000 series CLBs. **(4M)**