Reg.No.									

INTERNATIONAL CENTRE FOR APPLIED SCIENCES

(Manipal University)

III SEMESTER B.S. DEGREE EXAMINATION – OCT. / NOV. 2017

SUBJECT: COMBINATIONAL AND SEQUENTIAL LOGIC (EC 231)

(BRANCH: CS/CE/MET/E&E/E&C)

Friday, 10 November 2017

Time: 3 Hours **Max. Marks: 100**

- ✓ **Answer ANY FIVE full Questions.**
- ✓ **Missing data, if any, may be suitably assumed**

1A) Using Quine Mccluskey method, Obtain the minimal sum

$F(A,B,C,D) = \sum m(0,1,5,7,8,10,14,15)$

1B) Expand A+BC'+ABD'+ABCD to minterms. Simplify the expanded minterms using karnaugh map and draw the circuit for the simplified expression using NAND gates. Also determine the essential prime implicant.

1C) Write a dataflow VHDL code for 1:4 demultiplexer **(10+5+5)**

2A) Simplify the following Boolean expression algebraically

(i) AB'C+B+BD'+ABD'+A'C (ii) (A+B).(A+C')+A'B'+A'C'

2B) Simplify the following function using 3 variable VEM technique

$F(A,B,C,D)=\sum m(2,3,5,6,8,11,12,13)$

2C) (i) Add 679.6 + 536.8 in BCD number system

(ii) Convert the following to the indicated bases $(3A9E.B0D)_{16} = (\ ?\ )_2 = (\ ?\ )_8$

(iii) Define the term sensitivity list in VHDL

(iv) Derive a logic expression that equals 1 only when the two bit binary numbers A_1A_0 and B_1B_0 have the same value. Draw the logic diagram and construct the truth table to verify the logic. **(5+5+10)**

3A) Design a combinational circuit to convert 8421 BCD to 2421 BCD using basic gates.

3B) Implement the following function using PLA $F_1=\sum m(0,2,4,6,7,8)$ $F_2=\sum m(10,12,13,15)$

3C) Implement the following multiple output combinational circuit using 4 to 16 decoder with active low outputs.

$F1=\sum m(1,2,4,7,8,11,12,13)$ $F2=\sum m(2,3,9,11)$ $F3=\sum m(10,12,13,14)$ $F4=\sum m(2,4,8)$

3D) Write a behavioral VHDL code for 8:1 multiplexer **(5+5+5+5)**

4A) Implement the following function F(A,B,C) = AB+B'C using (i) 4:1 multiplexer and basic gates (ii) 2:1 multiplexer and basic gates.

4B) Design a circuit for 4 to 2 priority encoder using basic gates

4C) Explain the operation of a master slave SR flipflop with a neat circuit diagram

4D) Design a mod 10 ripple up counter using T flipflop **(5+5+5+5)**

5A) Design a synchronous J-K counter that goes through states 3,4,6,7 and 3,….Is the counter self starting. Modify the circuit such that whenever it goes to an invalid state it comes back to state 3

5B) Derive the characteristic equation of JK flipflop and convert JK to SR flipflop

5C) Draw the logic diagram of JK flipflop using NAND gates. Derive the truth table for the same and explain its operation **(10+5+5)**

6A) Design a Mealy type Sequence detector to detect an overlapping sequence "1010"
6B) Explain the operation of 4 bit Ring counter with a neat circuit diagram and suitable timing waveforms
6C) Write the behavioral VHDL code for JK flip flop using if statement **(10+5+5)**

7A) Design a 3 bit synchronous up / down counter using JK flipflops
7B) With a neat circuit diagram, Explain the operation of 4 bit Universal Shift Register

S_1	S_0	Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

(10+10)

8A) Write the behavioral VHDL code for 4 bit binary parallel adder / subtractor
8B) Reduce the following state table and draw reduced state diagram

Present State	Next State X=0	Next State X=1	Output X=0	Output X=1
A	E	D	0	1
B	F	D	0	0
C	E	D	0	1
D	F	D	0	0
E	C	F	0	1
F	B	C	0	0

8C) Define the following and give one example for each
(i) Weighted codes
(ii) Self complementing codes
(iii) Gray codes

(10+4+6)