INTERNATIONAL CENTRE FOR APPLIED SCIENCES

(Manipal University)

III SEMESTER B.S. DEGREE EXAMINATION – OCT. / NOV. 2017

SUBJECT: ELECTRONIC DEVICES AND CIRCUITS (EC 232)

(BRANCH: EC and EE)

Monday, 6 November 2017

Time: 3 Hours **Max.Marks: 100**

- ✓ **Answer ANY FIVE full Questions.**
- ✓ **Missing data, if any, may be suitably assumed**

1A. Design a Zener diode shunt regulated power supply with following specifications a) O/p voltage is 10V. b) Load current is 50mA c) Maximum power dissipation of 500mw and d) Input voltage is $15 \pm 2V$

1B. Draw the circuit of negative and positive clamper and explain its operation with the input and output waveform. (10+10)

2A. For a full wave rectifier using center tapped transformer, derive a) Ripple factor b) The average value of load current c) The rms value of load current d) Efficiency of the rectifier.

2B. Explain with a neat circuit diagram and waveforms, how transistor can be used as switch .

2C. In a transistor, 99% of the carriers injected into the base cross over to the collector region. If collector current is 4mA and collector leakage current is 6 μA, calculate emitter and base currents. (10+6+4)

3A.What is the drawback of fixed bias? How do you overcome it? Explain with neat circuit diagram the modified biasing circuit.

3B. Explain with neat circuit diagram RC-coupled amplifier. Discus the use of all the components in the circuit and why they are used. Also draw the frequency response of the amplifier. (10+10)

4A. Explain the construction, working and characteristics of enhancement P- MOSFET.

4B. What is Barkhausen criteria? Write the circuit of Hartley oscillator and explain its working. (10+10)

5A. Derive an expression for efficiency of Class B power Amplifier.

5B. Compare class A, B, C and D amplifier (10+10)

6A. Determine V_O for the network shown in Fig Q6A for the input indicated. Show the steps involved.

6B. For the circuit shown in Fig Q6B, determine I_{BQ}, I_{CQ}, V_{CEQ}, V_C, V_E, V_B. Draw the load line. (10+10)

7A. Explain how CMOS can be used as a NOT gate. What are the advantages of the CMOS?

7B. Sketch the transfer characteristic of a P-channel JFET device with I_{dss}=4 mA and V_p=3V

7C. Compare FET and BJT. (10+6+4)

8A. Explain the operation of PN junction diode along with diode current equation and V-I characteristics under different bias conditions.

8B. Draw the circuit of Emitter follower. What are the advantages of emitter follower?

(10+10)

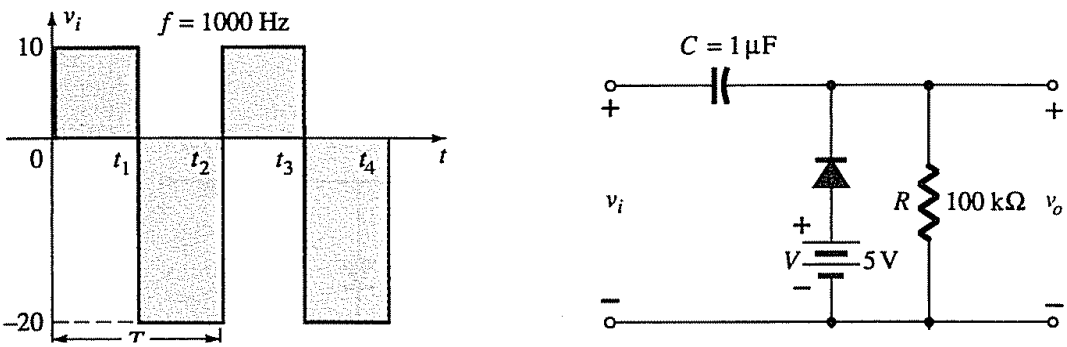

Fig Q6A.

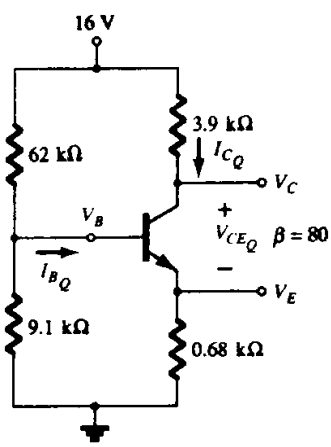

Fig.Q.6B