Reg.No.									

INTERNATIONAL CENTRE FOR APPLIED SCIENCES

(Manipal University)

IV SEMESTER B.S. DEGREE EXAMINATION – OCT. / NOV. 2017

SUBJECT: COMPUTER ARCHITECTURE (CS 242)

(BRANCH: CS and CE)

Saturday, 11 November 2017

Time: 3 Hours **Max. Marks: 100**

- ✓ **Answer ANY FIVE full Questions.**
- ✓ **Missing data, if any, may be suitably assumed.**

1A. Explain the following:
- i. Difference between computer architecture and organization
- ii. On board cache
- iii. Branch prediction
- iv. Data flow analysis
- v. Speculative execution

1B. Explain the key characteristics of a computer memory system.

(10+10)

2A. Write the salient features of RAID levels 2,3,4,5 and 6.

2B.
- i. Draw and explain the Winchester Disk Format (Seagate ST506).
- ii. With neat diagram explain typical cache organization.

(10+10)

3A.
- i. With necessary diagram explain how a virtual address is mapped to a physical address using paging.
- ii. Explain associative memory Translation Look-aside Buffer with diagram.

3B. Explain the following addressing modes with figures.
- i. Stack
- ii. Register
- iii. Displacement
- iv. Indirect
- v. Immediate

(10+10)

4A.
- i. Write the Pentium instruction format and explain the following fields:
  - a) Instruction prefix
  - b) ModR/M
- ii. Explain different categories of user visible registers of CPU.

4B. With neat diagram explain data flow during fetch, indirect, execute and interrupt cycle.

(10+10)

5A.
- i. With neat diagram explain two address field sequencing technique in the case of micro instructions.
- ii. With neat diagram describe the hardwired implementation of the control unit.

5B. Distinguish between hardwired and micro-programmed control unit. Explain the functioning of micro programmed control unit with a neat figure.

(10+10)

6A. i. Draw the flow chart for Booths algorithm. Multiply (8) x (-5) using this algorithm.

ii. Explain floating point division with a neat flow chart

6B. Explain 32 bit IEEE floating point format. Represent the following in this format.

i. 2.6875

ii. -1/16

(10+10)

7A. i. Briefly explain isolated verses memory mapped I/O.

ii. Explain DMA controller with a neat block diagram.

7B. i. With diagram explain the Daisy-Chain priority interrupt

ii. Write short notes on SISD and MIMD architectures.

(10+10)

8. Write short note on:

a) Time shared common bus
b) Parallel arbitration logic
c) Cross bar switch
d) Serial arbitration procedure
e) Multiport memory

(20)