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# INTERNATIONAL CENTRE FOR APPLIED SCIENCES

(Manipal University)

## IV SEMESTER B.S. DEGREE EXAMINATION – OCT. / NOV. 2017

**SUBJECT: ELECTRONIC DEVICES AND COMPUTER INTERFACING (CS241)**

**(BRANCH: CS)**

**Friday, 03 November 2017**

**Time: 3 Hours** **Max. Marks: 100**

- ✓ **Answer ANY FIVE full Questions.**
- ✓ **Missing data, if any, may be suitably assumed**

1A. Draw the circuit diagram of common emitter NPN transistor configuration. Plot and explain the input and output characteristics of it.

1B Draw the circuit diagram of an RC coupled amplifier using NPN transistor. Mention the role of each component. Sketch the frequency response. Indicate its salient features.

(10+10)

2A Derive the expression for output voltage of a typical instrumentation amplifier with a neat circuit diagram. If $R_1$ = 10kΩ, $R_2$ = 20kΩ, $R_3$ = $R_4$= 10kΩ, $V_1$ = 2V and $V_2$ = 3V, find the output voltage.

2B With a neat circuit diagram, relevant waveforms and expressions explain the working of a triangular wave generator.

(10+10)

3A Draw the physical structure of an n-channel enhancement-type MOSFET and explain the working of it in different operating regions.

3B Plot and explain the VI characteristic of n-channel depletion-type MOSFET.

(10+10)

4A With a neat circuit diagram and relevant waveforms explain the working of an Astable multivibrator using 555 timer. Give the expression for time period of the wave.

4B With a neat block diagram derive the expression for closed loop gain of a general oscillating circuit and discuss the Barkhausen Criterion required for oscillations.

(10+10)

5A A Si Transistor is biased in voltage divider bias circuit has $R_1$ = 47KΩ, $R_2$ = 15KΩ, $R_C$ = 1.5KΩ, $R_E$ = 1KΩ, β=50 and $V_{CC}$ = 15V. Draw the circuit diagram. Compute $V_{CE}$, $I_C$, $V_B$ and $V_C$.

5B With a neat circuit diagram derive the output voltage expression for an op-amp inverting adder. Design an op-amp circuit using inverting adders such that output is given by $V_0$ = 0.75 $V_1$ - 0.5 $V_2$ +0.25 $V_3$, where $V_1$, $V_2$ and $V_3$ are input voltages. Select $R_F$ = 10 kΩ.

(10+10)

6A A half wave rectifier circuit is fed by 230V, 50Hz ac at the primary of a transformer having turns ratio of 20:1, and has a load of 1kΩ. Draw the circuit diagram. Derive the expression and calculate its value for dc output voltage, rms output voltage and efficiency. Assume ideal diodes.

6B What is load regulation? A Zener diode regulates at 10V with maximum diode current of 40mA. The input voltage Vi = 50V. Calculate the series resistance Rs and range of load resistance $R_L$ to allow voltage regulation from a load current $I_{Lmin}$= 0 to $I_{Lmax}$ = 30mA. Draw the circuit diagram.

(10+10)

7A Explain the working of a dual slope ADC with a neat block diagram and slope plot.

7B Draw the VI characteristics of a SCR and explain the same.

(10+10)

8A The reverse saturation current of a silicon diode is 20nA at $17^0$C. At $27^0$C when it is forward biased by 0.5V, find

i) Diode current

ii) Dynamic forward resistance.

iii) Diode voltage required to get 20mA current.

8B Draw the circuit diagram and with relevant waveforms explain the working of

i) A clipper which clips the positive peak of input waveform at +2V.

ii) A clamper with output voltage positive peak as +2V.

Consider an input sinusoidal signal Vin = 10 sin ωt is applied. Assume ideal diodes.

(10+10)