Reg. No.										

INTERNATIONAL CENTRE FOR APPLIED SCIENCES

(Manipal University)

IV SEMESTER B.S. DEGREE EXAMINATION – OCT. / NOV. 2017

SUBJECT: VLSI DESIGN (EC 245)

(BRANCH: E & C)

Tuesday, 07 November 2017

Time: 3 Hours **Max. Marks: 100**

- ✓ **Answer ANY FIVE FULL Questions.**
- ✓ **Layout must be drawn using the graph sheet provided.**
- ✓ **Missing data may be suitably assumed.**

1A. Derive the relationship between drain to source current I_{ds} and voltage V_{ds} when MOS device is operated in resistive and saturation region.

1B. Prove that an inverter driven through one or more pass transistors should have $Zp.u/Zp.d$ ratio of $\geq 8/1$.

(10+10)

2A. (i) State Moore's Law and explain its significance in VLSI.
(ii) Discuss about technology evolution from Small Scale Integration to Super large Scale Integration.

2B. With neat figures explain the different steps involved in the fabrication of CMOS inverter using SOS technique. State the merits and demerits of SOS technique.

(10+10)

3A. Draw the stick notation and Layout for two way data selector with enable control input.

3B. Find the optimal number of NMOS inverters to be cascaded so as to drive load capacitance of 0.54 pF off-chip capacitive load such that the total delay is minimized. Given that 1□Cg = 0.01pF. Give the cascaded structure with L: W ratios shown. Find the overall delay showing the delay T_d across each inverter stage.

(10+10)

4A. Explain the working of Direct coupled FET Logic (DCFL) inverter. Draw its transfer characteristics.

4B. Explain the second order effects of MOSFET in detail.

(10+10)

5A. Give hardware implementation for storing following 4-bit words using NMOS ROM structure. word1: 0101 ; word2: 0010 ; word3: 1001 ; word4: 0110

5B. Give the circuit implementation of following multiple output function using NMOS based PLA. Give the stick notation. $Z_1 = AB + \bar{A}\bar{B}C$; $Z_2 = AB$; $Z_3 = A + \bar{B}C$

(10+10)

6A. Discuss the structured design implementation of (N+1)-bit parity indicator block that is provided with $n+1$ bit input word $A_n A_{n-1} A_{n-2} \ldots A_1 A_0$. The circuit has one bit parity output P. P will be HIGH (LOW) for even (odd) number of 1s at input. Give the stick notation for CMOS implementation of standard cell.

6B. Explain the operation of inverting and non- inverting super buffer. How does super buffer avoid unequal rise and fall delay in NMOS inverters. Give proper justification. (10+10)

7A. Design the circuit of **Figure 7A** so that transistor operates at I_D= 0.4mA and V_D = 0.5V.The NMOS transistor has V_t= 0.7V, $\mu_n C_{ox}$ = 100 µA/V^2, L= 1µm and W= 32µm.Neglect the channel length modulation effect.

7B. Explain different scaling models. Discuss the effect of different scaling on following parameters:
[i] Gate area A_g [ii] Gate capacitance per unit area C_o [iii] Carrier density in channel Q_{on}
[iv] Maximum operating frequency f_o.

(10+10)

8A. (i) Implement $\boldsymbol{F} = [\boldsymbol{A}.(\boldsymbol{B}+\boldsymbol{C})+(\boldsymbol{D}.\boldsymbol{E})]'$ using Dynamic CMOS logic.
(ii) Implement $\boldsymbol{F} = [(\boldsymbol{A}+\boldsymbol{B}).(\boldsymbol{C}+\boldsymbol{D}).(\boldsymbol{E}+\boldsymbol{F}+(\boldsymbol{G}.\boldsymbol{H}))]'$ using CMOS logic.

8B. (i) According to Moore's first law the number of …… in an ……. doubles approximately every two years.
(ii) The MOS device is characterised by ……whereas BJT is characterised by……
(transconductance, output conductance, current gain)
(iii)……. device offers lower resistance. (NMOS/ PMOS)
(iv)MOSFET is more noiser than BJT. The statement is …… (True/ False)
(v) The …….type of MOSFET is normally ON device and ……type of MOSFET is normally OFF device.
(vi)In Twin tub, both an N-well and a P-well are manufactured on a lightly doped N-type substrate.
(True/ False)
(vii) Fermi potential Φ_F is positive for NMOS and negative for PMOS. (True/ False)
(viii) Source to bulk potential V_{SB} positive for PMOS and negative for NMOS. (True/ False)
(ix)In a MOSFET, the polarity of the inversion layer is the same as that of the majority carries in the substrate. (True/ False)
(x) Channel current reduces on application of a more positive voltage to the gate of the depletion mode n-channel MOSFET. (True/ False) (10+10)

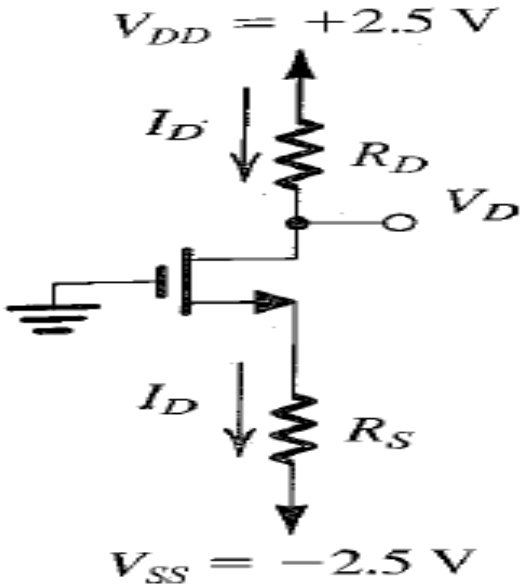

Figure 7A