Reg. No. | | | | | | | | | | |

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

III SEMESTER B.Tech.(BME) DEGREE MAKE UP EXAMINATIONS DEC 2017

SUBJECT: DIGITAL ELECTRONICS (BME 2103)

(REVISED CREDIT SYSTEM)

Thursday 28th December 2017: 9AM to 12 NOON

TIME: 3 HOURS **MAX. MARKS: 100**

Instructions to Candidates:

1. Answer all FIVE full questions. 2. Draw labeled diagram wherever necessary.

1. (A) (i) A gate is required to monitor two lines and to generate a HIGH level output used to activate an electric motor whenever either or both lines are LOW. Sketch the operation. 06

(ii) A certain application requires that two lines be monitored for the occurrence of a HIGH level voltage on either or both lines. Upon detection of a HIGH level, the circuit must provide a LOW voltage to energize a particular indicating device. Sketch the operation.

(iii) A certain system contains two identical circuits operating in parallel. As long as both are operating properly, the outputs of both circuits are always the same. If one of the circuits fails, the outputs will be at opposite levels at sometime. Devise a way to detect that a failure has occurred in one of the circuits.

(B) What is a digital comparator? Design a 2-bit digital comparator using logic gates. 08

(C) Design an 4-bit binary parallel adder/subtractor with a control input to select between addition and subtraction. 06

2. (A) What is a Multiplexer? Design the following using Multiplexers. 08

(i) Full adder using 8:1 Multiplexers.

(ii) 3-bit binary to gray code converter using 4:1 Multiplexers.

(B) Obtain the minimum sum of products (SOP) expression using Karnaugh map for each of the following Boolean expressions. 06

(i) $F = \bar{A}\bar{B}\bar{C} + A\bar{C}\bar{D} + A\bar{B} + ABC\bar{D} + \bar{A}\bar{B}C$

(ii) $F = \bar{A}\bar{B}\bar{D} + A\bar{C}\bar{D} + \bar{A}B\bar{C} + AB\bar{C}D + A\bar{B}C\bar{D}$

(C) A combinational circuit is defined by the following three functions: 06

$F_1 = \bar{x}\bar{y} + xy\bar{z}$ $F_2 = \bar{x} + y$ $F_3 = xy + \bar{x}\bar{y}$

Design the circuit with a 3 to 8 line decoder and suitable gates.

3. (A) Minimize the following Boolean expressions using Boolean algebra techniques. 04

$(i)\ Y = \bar{A}B + A\bar{B} + AB$

(ii) $Y = B\bar{C}\bar{D} + \bar{A}BD + ABD + BC\bar{D} + \bar{B}CD + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}D$

(B) What is the difference between common anode and common cathode type of 7-segment displays? Design a decoder/driver circuit for the common cathode type of 7-segment display, to display the decimal numbers from 0 to 3. 08

(C) Explain the function table associated with a 4-bit universal bidirectional shift register – IC 74194. Design a 4-bit Johnson counter using IC 74194 and suitable gates. 08

4. (A) Construct the state diagram for a Moore sequential circuit that will detect an non-overlapping sequence "1010" from an input sequence. 04

(B) (i) Design a decade ripple counter using JK Flip-flops. Illustrate its working using the timing diagram. 08

(ii) A decade ripple counter uses Flip-flops with a propagation-delay of 20ns each. What will be the maximum time required for change of state?

(iii) The output frequency of a decade counter is 6kHz. What is its input frequency?

(C) (i) Perform the following decimal additions in the 8421 code. 08

(a) 88.6 + 12.3 (b) 679.6 + 536.8

(ii) Perform the following subtractions using 1's and 2's complements:

(a) 11010_2 - 1101_2 (b) 100_2 - 11000_2

(iii) Solve the following equation for *x*:

$x_{16} = 1111\ \ 1111\ \ 1111\ \ 1111_2$

(iv) What range of decimal values can be represented by a 4-digit octal number?

5. (A) Why synchronous counters are faster than ripple counters? Design a 3-bit synchronous counter using D Flip-flops. 06

(B) Realize a one digit BCD adder using 7483 ICs. Describe how the BCD adder circuit detects the need for a correction and executes it. 06

(C) Design a Mealy sequential circuit using JK flip-flops, which detects an overlapping sequence 1010 from an input sequence. 08