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# MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
*A Constituent Institution of Manipal University*

**III SEMESTER B.Tech.(BME) DEGREE END SEM EXAMINATIONS NOVEMBER 2017**
**SUBJECT: DIGITAL ELECTRONICS (BME 2103)**
(REVISED CREDIT SYSTEM)
**Thursday, 23rd November 2017: 9AM to 12 NOON**

**TIME: 3 HOURS** **MAX. MARKS: 100**

**Instructions to Candidates:**

**1. Answer all FIVE full questions. 2. Draw labeled diagram wherever necessary.**

1. (A) A switching circuit has two control inputs ($C_1$ & $C_2$), two data-inputs ($X_1$ & $X_2$), and one output (Z). The circuit performs logic operations on the two data-inputs, as shown in the table. The logic operations performed depends on the control inputs. 06

| $C_1$ | $C_2$ | Logic operation performed by the circuit |
|---|---|---|
| 0 | 0 | OR |
| 0 | 1 | XOR |
| 1 | 0 | AND |
| 1 | 1 | MAGNITUDE COMPARISON |

(a) Derive the truth table for the output Z. (b) Use a K-Map to find the minimum gate-circuit to realize Z.

(B) What is a digital comparator? Design the following digital comparators: 08

(a) 1-bit comparator using logic gates.

(b) 5-bit comparator using a 4-bit comparator (IC 7485) and suitable gates.

(C) Design an 8-bit binary parallel adder/subtractor with a control input to select between addition and subtraction. 06

2. (A) What is a full adder? Design a full adder circuit using each of the following: 08

(a) 8:1 Multiplexers, and (b) 4:1 Multiplexers

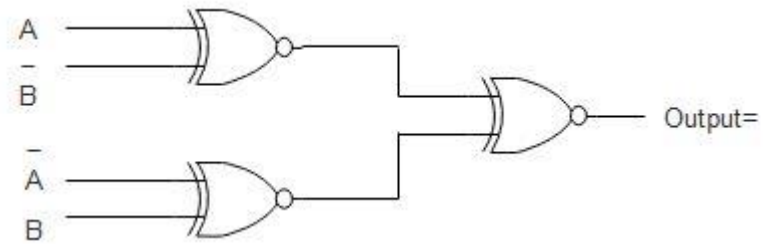
(B) Obtain the minimum sum of products (SOP) expression using Karnaugh map for each of the following Boolean functions. 06

(a) $f(A,B,C,D) = \sum m\,(0,2,4,5,6,7,8,10)$

(b) $f(A,B,C,D) = \sum m\,(1,8,12,13) + \sum d\,(3,\ 7,\ 10,11,14,15)$ $\quad d \rightarrow$ don't cares

(C) Design an Excess-3 to BCD code converter using 4 to 16 line decoder and additional gates. 06

3. (A) Calculate the output of the following logic circuit using Boolean algebra techniques. 04




(B) What is the difference between common anode and common cathode type of 7-segment displays? Design a decoder/driver circuit for the common cathode type of 7-segment display, to display the decimal numbers from 0 to 7. 08

(C) Explain the function table associated with a 4-bit universal bidirectional shift register – IC 74194. Construct a 4-bit Ring counter using IC 74194 and suitable gates. 08

4. (A) Construct the state diagram for a Mealy sequential circuit that will detect a sequence "1100" from an input sequence. 04

(B) (i) Design a 4-bit ripple counter using JK Flip-flops. Illustrate its working using the timing diagram. 08

(ii) A 4-bit ripple counter uses Flip-flops with a propagation-delay of 25ns each. What will be the maximum time required for change of state?

(iii) The output frequency of a Mod-12 counter is 6kHz. What is its input frequency?

(C) (i) Perform the addition of the following BCD numbers: 08

(a) 0110 0111 and 0101 0011, (b) 0100 0100 1000 and 0100 1000 1001

(ii) A computer system uses a 20-bit address code to identify each of over 1 million binary locations. How many hex-characters are required to identify the address of each memory location? What is the hex-address of the $200^{th}$ memory location?

(iii) Digital thermometers use BCD to drive their digital displays. How many BCD bits are required to drive a 2-digit thermometer display? What are the BCD bits sent to the display, to display the temperature $97^{o}$C?

(iv) What range of decimal values can be represented by a 4-digit hex number?

5. (A) What is the advantage of a synchronous counter over a ripple counter? Design a 3-bit Gray-code synchronous counter using JK Flip-flops. 06

(B) Using a suitable IC (and gates), design a circuit to subtract 1001 from 1101, using the following methods: (a) 1's complement subtraction, and (b) 2's complement subtraction 06

(C) Design a Moore sequential circuit using D flip-flops, which detects an overlapping sequence 101 from an input sequence. 08