Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
A Constituent Institution of Manipal University

III SEMESTER B.TECH (COMPUTER SCIENCE AND ENGINEERING)

MAKEUP EXAMINATIONS, NOV/DEC 2017

SUBJECT: COMPUTER ORGANIZATION AND DESIGN [CSE 2101]

REVISED CREDIT SYSTEM

Time: 3 Hours **20-12-2017** MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** questions.
- Missing data, if any, may be suitably assumed.

1A. Explain the levels in which parallelism can be implemented? **2M**

1B. Consider **5M**

X =	0	10001010	00100101001001000000000
Y=	0	01111110	10000000000000000000000

and perform the following

(a) Perform addition of X and Y and obtain the sum.
(b) Normalize the sum if necessary.
(c) For the above obtained sum apply rounding technique to truncate the result to10 bits.
(d) Represent the sum after rounding in IEEE floating point format.

1C.Design a 16-bit carry look ahead adder using 4-bit CPA as building blocks. Calculate the delays for c13 and s13. **3M**

2A.Consider the state diagram given below in figure 2A. Draw the hardwired controller and also draw the truth table. **5M**

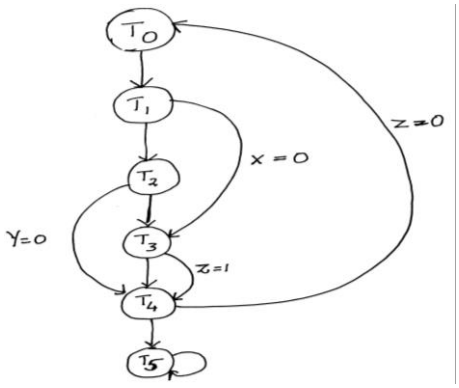

Figure 2A

2B. What are the rules of detecting overflow in two's complement numbers? Explain each with an example. **3M**

2C.Explain all the addressing modes used in RISC. Also mention how effective address is calculated in each of the addressing mode. **2M**

3A. Assuming that the memory is byte addressable. Fill in the blanks given in the Table 3A. Use direct mapping technique . **4M**

Main Memory size	Cache size	Block size	Tag bits
128KB	16KB	256B	----------
32GB	32KB	1KB	----------
----------	512KB	1KB	7
16GB	----------	4KB	10

Table 3A

3B. How performance of memory is enhanced in virtual memory? Justify the same with a neat diagram and also explain the address translation mechanism followed? **3M**

3C. Multiply the following pairs of signed 2's-complement numbers using :(i) Booth algorithm (ii) Bit-pairing of the multiply A = 010111 and B = 110110. Assume A is the multiplicand and B is the multiplier . **3M**

4A. Draw the processing section for the below register transfer notation given. **4M**

Declare registers A[4], B[4], C[4], D[4];
Declare bus inbus1[4], inbus2[4],outbus[4];

Start: A ← 0,B←inbus1, C←4,D←inbus2;
Loop: if A[0]=0 then
A←B+D;
If A[0]=1 then
A← B-D;
Go to decrement
Decrement: C←C- 1;
If C > 0 then go to Loop
Outbus = A[4];
Outbus = B[4];
Halt: go to Halt;

4B. Consider a memory consisting of 64K words of 8 bits each. Give the organization to implement this memory using 16K X 1 static memory chips **4M**

4C. Explain with a neat diagram the connection between processor, keyboard and display. **3M**

5A. Suppose that a computer has a processor with two L1 caches, one for instructions and one for data, and an L2 cache. Let τ be the access time for the two L1 caches. The miss penalties are approximately 15τ for transferring a block from L2 to L1, and 100τ for transferring a block from the main memory to L2. For the purpose of this problem, assume that the hit rates are the same for instructions and data and that the hit rates in the L1 and L2 caches are 0.96 and 0.80 respectively. calculate the access time as seen by the processor. **4M**

5B.Explain briefly the following, use diagram wherever necessary
(i) Interrupts (ii) Direct memory Access. **4M**

5C. List out the difference between big endian and little endian assignment with a clear example. **2M**