Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

III SEMESTER B.TECH. (COMPUTER SCIENCE ENGINEERING)

END SEMESTER EXAMINATIONS, NOVEMBER 2017

SUBJECT: **COMPUTER ORGANIZATION AND DESIGN [CSE 2101]**

REVISED CREDIT SYSTEM
(16/11/2017)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitable assumed.

1A. i) With a neat sketch, discuss the connection between processor and main memory.
ii) Write short notes on supercomputers and grid computers. **3M**

1B. Write a RISC program to add two 3x3 matrices M1 and M2 and to store the result in matrix M3. Elements of M1 are stored in memory such that the consecutive elements of a row reside next to each other (row-major order), elements of M2 are stored in memory such that the consecutive elements of a column reside next to each other (column-major order) and M3 elements in row-major order. Each element occupies a word. Word length is 4 bytes and that the memory is byte addressable. **5M**

1C. Which is the best system to represent signed integers? Why? Represent -193 and +63 in that system using minimum number of bits. Subtract the second number from the first number using 10-bit addition. Has the result overflown? **2M**

2A. Draw the basic structure of a Full adder. Write the truth table for the same. Derive the Boolean equations for S_i and C_{i+1} from the truth table. Draw the circuits for S_i and C_{i+1}. Design a *n*-bit ripple carry adder using full adders. Design the cascade of *k n*-bit ripple carry adders. **4M**

2B. What is the minimum gate delay to find S62 in a 64-bit CLA constructed using 16-bit CLAs with carry propagation between the latter? Each 16-bit CLA is constructed using 8-bit CLAs with no carry propagation between the latter. Draw the above 64-bit CLA. **3M**

2C. Divide -145 by +13 using non-restoring integer division algorithm. **3M**

3A. Describe single precision and double precision floating point number systems. Represent +1.75 in single precision and +2.25 in double precision systems. **2M**

3B. Write the register transfer description for 5x5 bit-pair recoded multiplier. **4M**

3C. i) Design a 4-bit bidirectional data bus.
ii) Draw the state diagram and controller action (state table) for 4*4 booth multiplier. **4M**

4A. In the Figure Q.4A, determine the values to be given for J and K inputs of JK flip flops, if the timing signals are to be generated in the order T2, T1, T0 in successive clock cycles with T3 already generated.

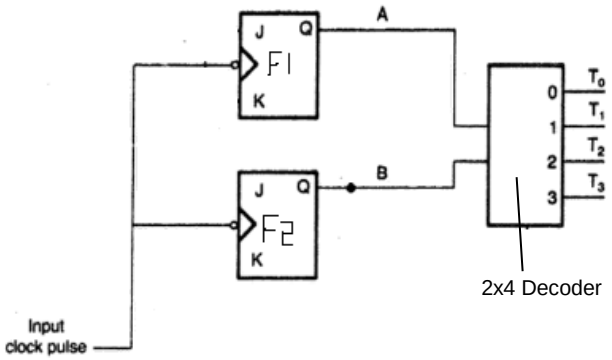

Fig. Q.4A **2M**

4B. i) Draw the architecture of a modern microprogrammed control unit.
ii) Discuss the 4 types of ROM. **4M**

4C. A byte-addressable computer has a small data cache capable of holding eight 32-bit words. Each cache block consists of one 32-bit word. When a given program is executed, the processor reads data sequentially from the following hex addresses:
200, 204, 208, 20C, 2F4, 2F0, 200, 204, 218, 21C, 24C, 2F4
This pattern is repeated four times.
i) Assume that the cache is initially empty. Show the contents of the cache at the end of each pass through the loop if associative-mapped cache that uses the LRU replacement algorithm is used.
ii) Assume that the cache is initially empty. Show the contents of the cache at the end of each pass through the loop if four-way set-associative cache that uses the LRU replacement algorithm is used. **4M**

5A. Describe virtual memory. Explain virtual memory address translation and TLB with a neat diagram for each. **5M**

5B. Define an interrupt. Discuss vectored interrupts and simultaneous requests. **3M**

5C. Explain the display to processor output interface with the help of a neat diagram. **2M**

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