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MANIPAL INSTITUTE OF TECHNOLOGY
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A Constituent Institution of Manipal University

III SEMESTER B.TECH. (COMPUTER SCIENCE AND ENGINEERING)
END SEMESTER EXAMINATIONS, NOV 2017
SUBJECT: SWITCHING CIRCUITS AND LOGIC DESIGN [CSE 2102]
REVISED CREDIT SYSTEM
(18/11/2017)

Time: 3 Hours Max. Marks: **50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A) Using the laws and theorems of Boolean algebra check whether the following expression is valid or not? (3M)

A'BD'+BCD+ABC'+AB'D=BC'D'+AD+A'BC

1B) Using functional decomposition find and draw the minimum cost circuit for the function **f (w, x, y, z) = ∑m (0, 4, 8, 13, 14, 15),** assuming that the inputs are available in un-complemented form only. What is the cost of this circuit? Compare this cost with the lowest cost SOP implementation? (4M)

1C) Simplify the function **f (A, B, C, D) = ∑m (0, 1, 2, 3, 4, 5, 7, 8, 10, 11, 15)** using K-map and draw the minimum cost **NOR** circuit assuming that the input variables are available only in un-complemented form and there is no fan-in restriction. (3M)

2A) Design a circuit to find the number of **1's** in a six-bit unsigned number using Full adder's and Half adder's**.** Explain the working of your design? (3M)

2B) Design a **2-bit** comparator circuit using 2-bit adder/subtractor. The inputs to the comparator are **A=a1a0** and **B=b1b0**, where A & B are signed numbers. The outputs are **A<B, A=B and A>B**. Write Verilog code for implementing this design. (4M)

2C) Design a full adder circuit using 2 input (3M)

i) **NAND** gates only

ii) **NOR** gates only

3A) Write the truth table for **4:2** priority encoder and its output equations. Write Verilog code to implement the same using **FOR** loop construct? (3M)

3B) What are the significance of "**blocking**" and "**non-blocking**" assignment statements in Verilog? Write Verilog code to implement two cascaded **D-FF's** with positive edge triggered clock. Draw the circuit defined as per your Verilog code. (3M)

3C) Design a **4-bit** register using **D-FF's** and **4:1** Multiplexer's that operate according to the following function given in table [Table Q3C], where S1 and S0 are the two control inputs. Explain the circuit functionality in brief. (4M)

Table Q3C

S1	S0	Register Operation
0	0	No change
0	1	Complement the outputs
1	0	Clears the register to 0
1	1	Load parallel data

4A) Draw the logic circuit of a **4-bit** parallel in, serial out shift register with a control input shift/$\overline{\text{load}}$ using D-FF's. When Shift/$\overline{\text{load}}$=0 parallel data will be loaded and when shift/$\overline{\text{load}}$ =1 serial shift will take place. Explain the functionality of this logic circuit. (3M)

4B) Using **RS-FF** draw the logic diagram of a **Master- Slave-FF** and explain its working with a sample waveform? (3M)

4C) Design a synchronous **BCD** down counter using **T-FF**? (4M)

5A) With necessary circuit diagram explain how **NMOS** transistor acts as a switch? Explain with circuit diagram the various transistor states of a **CMOS-NOR** gate? (5M)

5B) What are the drawbacks of **PLA's**? Design a **PAL** to realize the logic function **$f1=X_1X_2X_3'+X_1'X_2X_3$; $f2=X_1'X_2'+X_1X_2X_3$** and mention its advantages over **PLA's**? (3M)

5C) Define Noise margin? Write down the equations for low and high noise margins? (2M)