MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
A Constituent Institution of Manipal University

III SEMESTER B.TECH. (COMPUTER SCIENCE AND ENGINEERING)

MAKEUP EXAMINATIONS, NOVEMBER 2017

SUBJECT: SWITCHING CIRCUITS AND LOGIC DESIGN [CSE 2102]

REVISED CREDIT SYSTEM
(22/12/2017)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitable assumed.

1A Simplify the following expression using algebraic manipulation.
A'B+A'B'C'D'+ABCD' **3M**

1B Consider the function
F= $X_3X_5+X_1'X_2X_4+X_1X_2'X_4'+X_1X_3X_4'+X_1'X_3X_4+X_1'X_2X_5+X_1X_2'X_5$
Use factorization to derive minimum cost circuit that implements this function using only NAND gates. Assume that inputs are available in both complemented and un-complemented forms. **4M**

1C Find the minimum cost SOP expression for the function **F(w,x,y,z)=πM(2,3,6,8,9,11,12,13)** using k map. Write all prime implicants and essential prime implicants **3M**

2A Design a 4-bit arithmetic comparison circuit. Derive the expressions for A=B, A>B, and A>B, where A and B are 2 four bit numbers. **2M**

2B Write Verilog code for three bit multiplier using Half adder and full adder modules. **5M**

2C For the function f(x, y, z) = ∑m (0, 2, 3, 6) use Shannon's expansion to derive minimal cost implementation using 2 to 1 multiplexer and any other necessary gates. Assume that the inputs are available in un-complemented form only. Decompose f with respect to x, y and z to find where the cost is minimum. **3M**

3A Draw the circuits for the Verilog code segments a and b given below.

a)
```
always @ (posedge clock)
        begin
                f=a|b;
                g=f&c;
                h=g^d;
        end
```

b)
```
always @ (posedge clock)
        begin
                f<=a|b;
                g<=f&c;
                h<=g^d;
        end
```
2M

3B Explain the operation of a D-type positive edge triggered Flip-Flop using NAND gates with the logic diagrams for all the cases of D when CP=high. **4M**

3C Design a sequential circuit with two T flip flops A and B, and one input x, which functions as the following. When x=0 the state of the circuit remains the same. When x=1, the circuit goes through the state transitions from 00 to 01to 11 to 10 back to 00 and repeats. **4M**

4A Explain 4-bit Ring counter and Johnson counter with truth table and block diagram **3M**

4B Draw the logic diagram of a 4-bit register with 4 D-Flip Flops and four 4:1 multiplexers. Register operates according to the following function table given in table Q4B.

Table Q4B

S1	S2	Register Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Load parallel data

2M

4C Using JK flip-flops design a counter with the following repeated non binary sequence: 0,1,2,3,4,5,6. Treat the unused states as don't care conditions. Whether the final circuit is self-correcting or not? **5M**

5A With necessary circuit diagram explain how PMOS transistor acts as a switch? Explain with circuit diagram the various transistor states of a CMOS NAND gate? **4M**

5B What is a PLD? Explain the functionality of a PLA with a gate level diagram? **3M**

5C Mention the significances of static and dynamic power dissipation? Briefly explain how this is implied with NMOS and CMOS technology? **3M**