Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

III SEMESTER B.TECH. (COMPUTER AND COMMUNICATION ENGINEERING) MAKEUP EXAMINATIONS, DECEMBER 2017

SUBJECT: DIGITAL SYSTEM DESIGN [ICT 2151]

REVISED CREDIT SYSTEM
(22/12/2017)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer ALL the questions.
- Missing data, if any, may be suitably assumed.

1A.	Design a hardwired control unit for 4x4 Booth's multiplier.	5
1B.	Design a 1-bit magnitude comparator with cascading inputs. Using this, design a 2 - bit magnitude comparator.	3
1C.	Design a T flip flop from SR flip flop.	2
2A.	Design a synchronous sequential circuit, with one input A and one output Y. The output Y is to be HIGH whenever the sequence "10011" is detected. Otherwise the output is LOW. Overlapping of the sequence is allowed. Implement using T flip flops and external gates.	5
2B.	Given M= $17_{(10)}$ and Q= $-5_{(10)}$. Multiply using Booth's algorithm.	3
2C.	Design a 4:2 priority encoder.	2
3A.	Design a combinational circuit to evaluate the arithmetic expression $D = X^2 - Y^2$ using 7483IC and external gates, where X and Y are 2- bit binary numbers	5
3B.	With necessary diagrams, explain various cache mapping techniques.	3
3C.	Using 7490 ICs ONLY, design a logic circuit which divides the frequency of the input square wave by a factor of '100' and produces an output waveform with 50 percent duty cycle.	2
4A.	Design a code converter to convert a decimal digit represented in 2 4 2 1 to decimal digit represented in 8 4 2 1 code, using NOR gates only.	5
4B.	What is a race around condition? How is it overcome using master-slave configuration? Give necessary circuit diagrams and waveforms.	3
4C.	Design 5: 32 decoder using 3 to 8 decoders only.	2

5A. Design a self-starting synchronous counter using T flip flops and external gates to count the sequence 1 → 2 → 4 → 9 → 12 → 5 → 1 — 5

5B. Design a 3-bit carry look ahead adder. — 3

5C. Differentiate between restoring and non restoring division algorithms. — 2