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MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent Institution of MAHE, Manipal)

III SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

MAKE UP EXAMINATIONS, JANUARY 2018

SUBJECT: ANALOG ELECTRONIC CIRCUITS [ELE 2105]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 02 January 2018** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A For the circuit shown in fig Q1a, assuming ideal diodes, draw the transfer characteristic if Vi=25sinωt. (4)

1B For the circuit shown in fig Q1b, assuming constant voltage ($V\gamma$ = 0.7V) model for diode, draw the output waveform. Clearly show the calculation of output voltage during positive and negative half of input. (3)

1C With a neat circuit diagram discuss the working of Zener Voltage Regulator. (3)

2A What are the different regions of operation of MOSFET? Discuss with relevant expressions. (3)

2B Draw the MOSFET based RC coupled amplifier circuit diagram. Clearly state the role of circuit elements in defining *ac* and *dc* operation of the circuit. Also discuss the frequency response of this Amplifier, (5)

2C Define MOSFET pinch off. (2)

3A For the amplifier shown in Fig Q3a, $V_{TH} = 0.8\ V$, $\mu nCoxW/L=1mA/V^2$, $\lambda = 0$, V_{DD} = 10V, R_1=119kΩ, R_2= 281kΩ, I_{DQ}=1.5mA, Rsig=200Ω Determine Vo/Vin. Draw small signal model (4)

3B In the amplifier shown in fig Q3b, both the transistors are identical with $\mu_n C_{ox}W/L$ = 50mA/V², Vth = 2V, λ = 0.

i) Determine I_D, gm for both the transistors
ii) Draw the small signal model
iii) Find v_O/v_S.
iv) Find input resistance (Rin) and output resistance (Rout) (4)

3C State and prove Miller's theorem. (2)

4A For the circuit shown in fig Q4a, $Vthn = |Vthp| = 0.5$ V, $(\mu coxW/L)n$ = 100 μA/V² , $(\mu coxW/L)p$ = 60 μA/V² and $\lambda n = \lambda p = 0$. The quiescent values are V_O = 1.5 V and V_I = 1.2 V. Assuming M1 and M2 are matched

i) Determine the circuit W/L ratios, such that $I_{REF} = I_O$ = 100μA (4)
ii) Determine the small-signal voltage gain.

4B Prove that cascading of similar amplifier stages reduces overall bandwidth of resultant amplifier. (3)

4C Derive an expression for output resistance of a common Drain MOSFET configuration. (3)

5A For the series fed class A power amplifier, supply voltage V_{DD} = 10V, bias point V_{DS} = 4V, load resistance R_L = 10 Ω. Determine

(i) the bias current I_{DS}

(ii) the maximum peak to peak amplitude of a symmetrical output voltage if the minimum value of instantaneous drain to source voltage is equal to 0.5V

(iii) power conversion efficiency

(iv) transistor specifications. (4)

5B For the MOSFET based class – B complementary push pull power amplifier, evaluate the maximum efficiency. (3)

5C Derive an expression for CMRR of a Differential Amplifier (3)

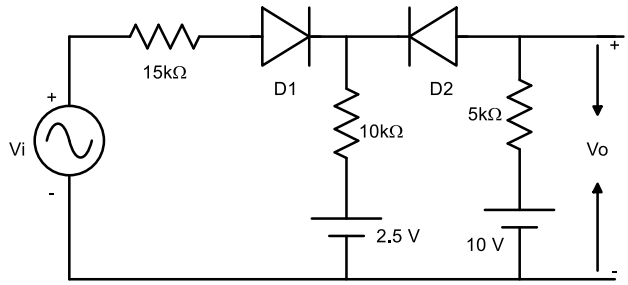

Fig Q1a

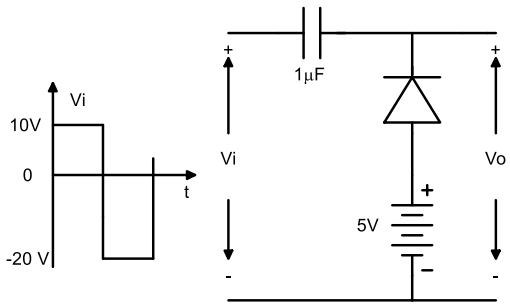

Fig Q1b

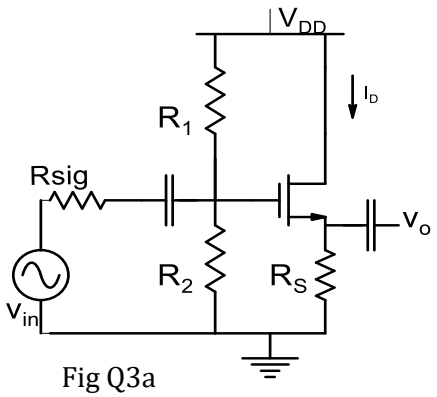

Fig Q3a

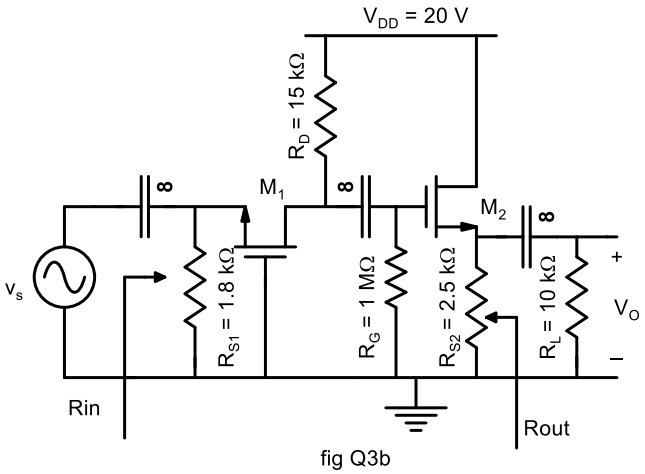

fig Q3b

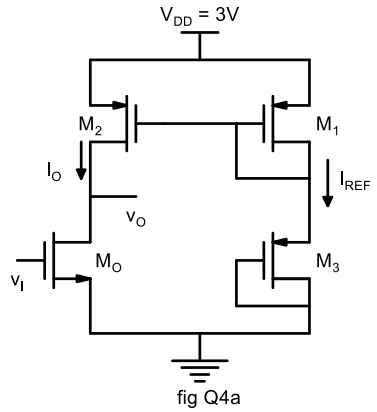

fig Q4a