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MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

III SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, NOVEMBER 2017

SUBJECT: DIGITAL ELECTRONIC CIRCUITS [ELE 2102]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 21 November 2017** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. For the given function $f(A,B,C,D)=\overline{A}\,\overline{D}+\overline{C}\,\overline{D}+A\overline{C}D+AC\overline{D}$.

i) Obtain the simplest Sum-of-Products expression
ii) Implement the function using minimum number of NAND gates.
iii) Implement the function using minimum number of NOR gates. ***(05)***

1B. Simplify the following equation using VEM technique. Take E as MEV.

f(A,B,C,D,E) = $\sum m(1,2,3,6,7,8,17,20,24,29)+d(5,10,11,12,14,15,16,21,25,28)$ ***(05)***

2A. Implement the function $f(A,B,C,D)=BD+\overline{B}C\overline{D}$ using

a) 8 to 1 Multiplexer/s
b) 3 to 8 decoder/s

Residual gates may be used ***(04)***

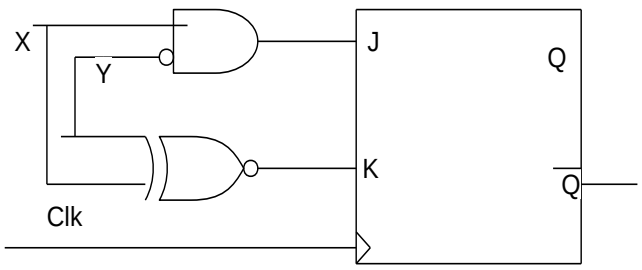
2B. Design Octal (0 to 7) to binary encoder circuit ***(03)***

2C. Design a comparator using 4 bit 74LS283 and residual gates that compares two 4 bit unsigned numbers,X_3-X_0 and Y_3-Y_0 .The comparator has two outputs G and S, Such that G=1 and S=0 if X>Y and S=1 and G=0 if X<Y and G=S=0 if X=Y ***(03)***

3A. An XY FF is constructed from JK FF as shown below

a) Write an expression for X and Y.

b) Derive the excitation table and characteristic equation for XY FF



(04)

3B. Design an asynchronous counter which counts from 5 to 12 using D flip flops. ***(03)***

3C. Design a sequence generator using 74LS194 IC (Universal Shift Register) to generate the following sequence 1110- 0111-1011-1101----. Repeats. ***(03)***

4A. Design a two-digit counter which counts from 00-88 using 74LS93. Assume that each digit will count from 0 to 8 only. ***(03)***

4B. A synchronous counter is controlled by two input signals A and B. The counter does not operate, if A=B. When A=0 and B=1, the counter operates as a mod 8 down counter. If A=1 and B=0 the counter operates as a mod 8 up counter. Draw an ASM chart to satisfy the above condition. ***(03)***

4C. A sequential circuit with two D Flip flops A & B, one input X and one output Z, is specified by the following equations.

$$D_A = x;\ D_B = Q_A + \bar{x};\ Z = \overline{Q}_A Q_B \bar{x} + Q_A Q_B x$$

1. Draw the logic diagram of the circuit
2. Derive the state table
3. Draw the state diagram
4. Identify the objective of the problem ***(04)***

5A. Design a linked state machine to detect the sequence 011 as a Moore machine, in a block of 100 bits. Use 7490 ICs and T flip flops for the design. ***(07)***

5B. Implement the expression F= A+ BC using CMOS logic. ***(03)***