



MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent Institution of MAHE, Manipal)

III SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)
MAKEUP EXAMINATIONS, DECEMBER 2017

SUBJECT: ELECTRICAL CIRCUIT ANALYSIS [ELE 2101]

REVISED CREDIT SYSTEM

Time: 3 Hours

Date: 20 December 2017

Max. Marks: 50

Instructions to Candidates:

- ❖ Answer **ALL** the questions.
- ❖ Missing data may be suitably assumed.

- 1A.** In the circuit shown in Fig Q1A, find voltage across $30\ \Omega$ resistor using Superposition Theorem. **05**
- 1B.** In the network shown in Fig Q1B, find the value of maximum power delivered to the load, if the load consists of variable resistance and reactance. **05**
- 2A.** In the circuit shown in Fig Q2A, R is varied from 0 to ∞ . Draw the locus of current ' I ' and hence determine
- i) Minimum current
 - ii) Maximum current
 - iii) Current at resonance
 - iv) Value of R at resonance
- 06**
- 2B.** In the network shown in Fig Q2B, switch is closed at $t = 0$. Find v_1 and dv_1/dt at $t = 0^+$. **04**
- 3A.** Decompose the signal shown in Fig Q3A into its even and odd component signals. **03**
- 3B.** In the network shown in Fig Q3B, switch has been closed for a long time. If it is opened at $t = 0$, draw the transformed network for loop current analysis and hence find $i(t)$. **04**
- 3C.** Draw the pole-zero diagram of the function
- $$V(s) = \frac{(s^2 + 4)}{s^3 + 3s^2 + 2s}$$
- Hence, obtain $v(t)$ from the pole-zero diagram. **03**
- 4A.** In the network shown in Fig Q4A, switch is closed at $t = 0$. Find expression for the voltage across capacitor for $t > 0$ using time domain analysis. **05**
- 4B.** In the network shown in Fig Q4B, switch is moved from position 1 to position 2 at $t = 0$. Switch was in position 1 for long time. Determine $i(t)$ for $t > 0$ using time domain analysis. **05**
- 5A.** Find the Y-parameters of the network shown in Fig Q5A. **05**
- 5B.** Decompose the network shown in Fig Q5B into 2 two-port networks in series and hence find overall Z-parameters. **05**

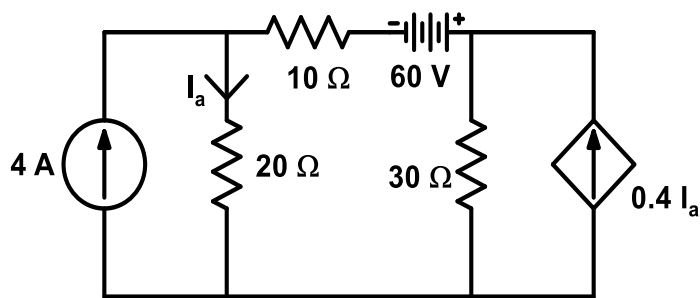


Fig Q1A

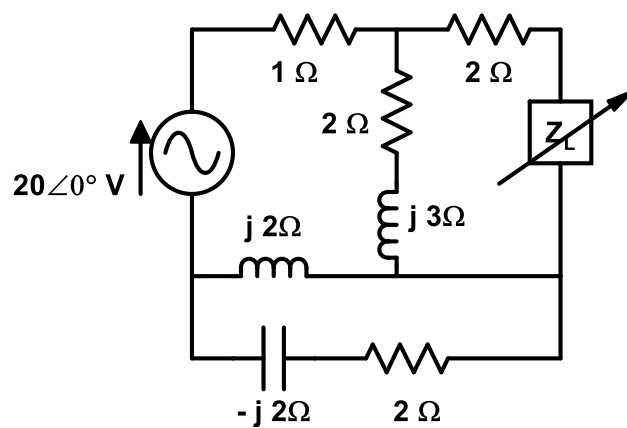


Fig Q1B

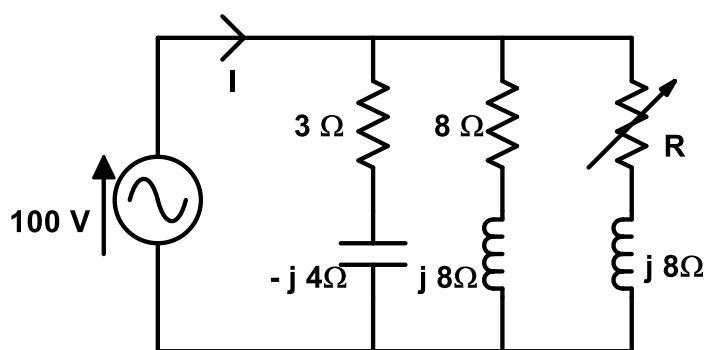


Fig Q2A

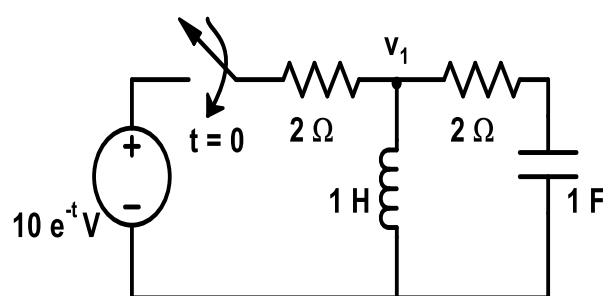


Fig Q2B

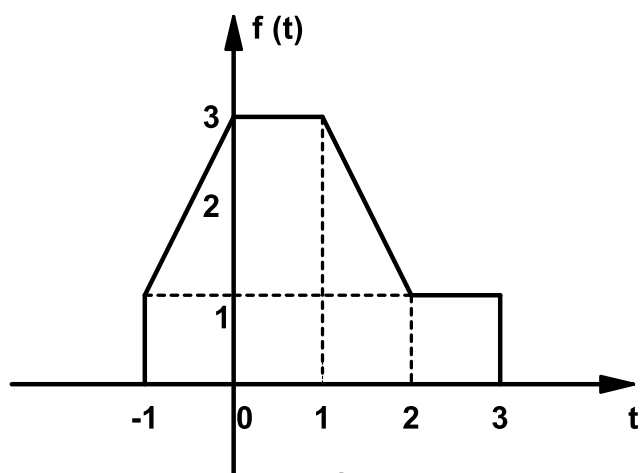


Fig Q3A

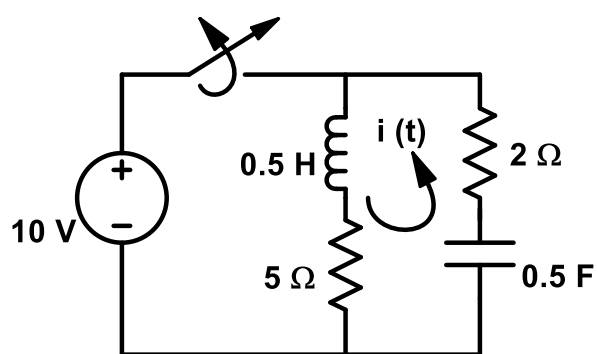


Fig Q3B

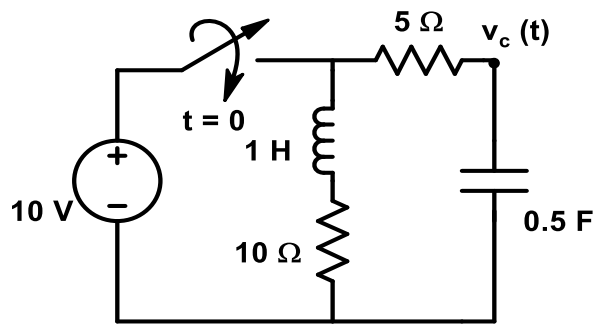


Fig Q4A

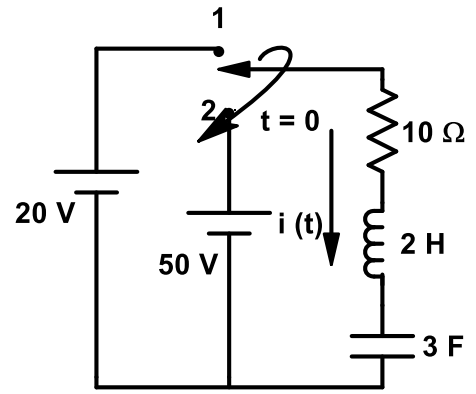


Fig Q4B

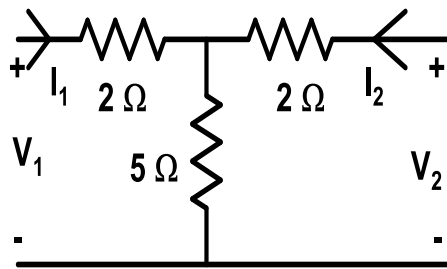


Fig Q5A

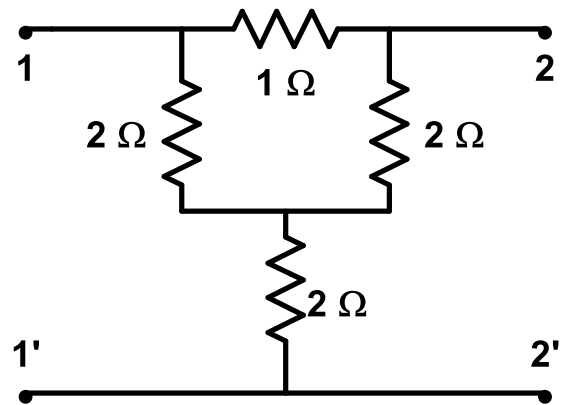


Fig Q5B