MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
A Constituent Institution of Manipal University

THIRD SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION
NOV/DEC 2017
SUBJECT: ANALOG ELECTRONIC CIRCUITS (ECE – 2101)

TIME: 3 HOURS MAX. MARKS: 50

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Design the CE stage of Fig. Q1(A) for a power budget of 1mW and a voltage gain of 20. Assume $\beta=100$, $V_A=\infty$ and $I_S=5x10^{-17}A$

1B. If a BJT in CE configuration is biased at a collector current of 1mA. Determine all small signal parameters. Assume $\beta=100$, $V_A=20V$ and $I_S=5x10^{-17}A$

1C. Compute the value of W/L for M1 in Fig.Q1(C). for a bias current of 1mA. Assume $\lambda=0$ and $R_s=200\Omega$.

(5+3+2)

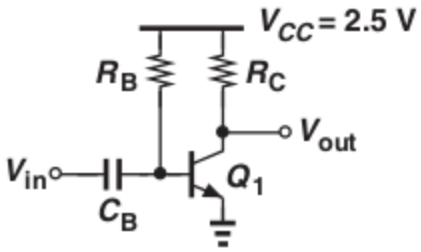

Fig.Q1(A)

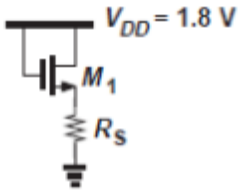

Fig Q1(C)

2A. The circuit of Fig. 2(A) must be designed for a voltage drop of 200mV across R_S . Assume $\mu_n C_{ox}=100\mu A/V^2$, $V_{th}=0.4V$ and $\lambda=0$.
(a) Calculate the minimum allowable value of W/L if M_1 must remain in saturation.

(b) What are the required values of R_1 and R_2 if the input impedance must be at least 30kΩ?

2B. For the circuit shown in Fig. 2(B), determine I/O impedance and voltage gain. Assume $I_D=2mA$, $\mu_n C_{ox}=100\mu A/V^2$ $V_{th}=0.4V$, $\lambda=0$, $W/L=20$, $R_D=500\Omega$ and $R_G=20k\Omega$.

2C. Draw the small signal equivalent circuit for the circuit shown in Fig. Q2(C).

(5+3+2)

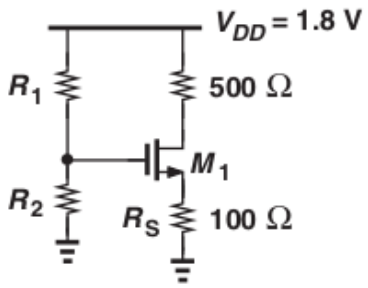

Fig Q2(A)

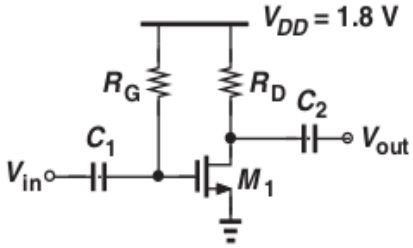

Fig. Q2(B)

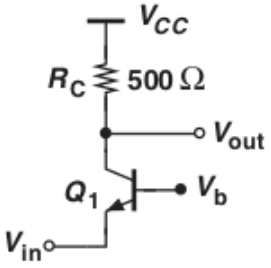

Fig Q2(C).

3A The circuit of Fig. Q3(A) is designed with W/L = 20/0.18, λ = 0, and I_D = 0.25 mA. (a) Compute the required gate bias voltage. (b) With such a gate voltage, how much can W/L be increased while M_1 remains in saturation? What is the maximum voltage gain that can be achieved as W/L increases. Assume $\mu_n C_{ox}$ =100μA/V^2 , V_{th}=0.4V.

3B. Explain the working of MOSFET as a voltage-dependent resistor. Also draw the I_D-V_D characteristics for various V_G.

3C. List the salient features of emitter follower.

(5+3+2)

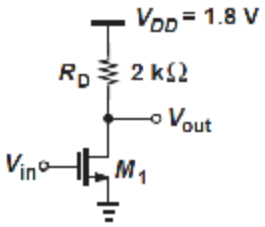

Fig.Q3(A)

4A. For the network of Fig. Q4(A),

(i) Obtain an expression for the transfer function of each stage.

(ii) Write the expression for the overall transfer function.

(iii) Obtain an expression for the oscillation frequency

(iv) To ensure oscillation start-up, obtain the condition on low-frequency gain of each stage

(v) If R_D = 2kΩ, and C_D = 0.1μF, at what frequency the circuit will oscillate?

4B. In the amplifier of Fig. Q4(B), $g_m = (150Ω)^{-1}$, λ= 0, R_D = 2kΩ, R_S = 200Ω, C_{in} = 1μF, and C_L = 43nF. Neglecting all other capacitors, plot the frequency response and calculate the cutoff frequency.

4C. In the amplifier of Fig. Q4(C), with λ > 0, with all other capacitances neglected, derive the transfer function. If λ = 0, what mathematical operation can be performed using this circuit?

(5+3+2)

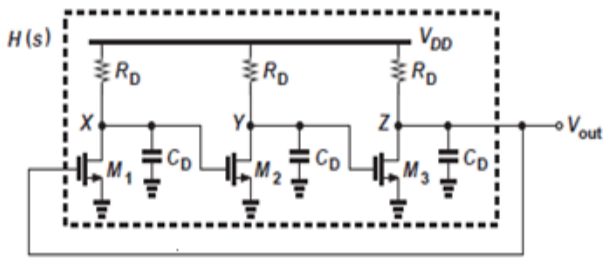

Fig. Q4(A)

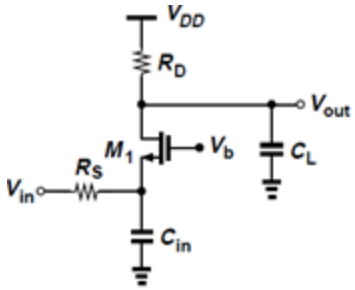

Fig. Q4(B)

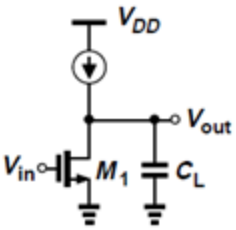

Fig. Q4(C)

5A. For the Push-Pull amplifier of Fig. Q5(A1) which has its V_{out} versus V_{in} plot as in Fig. Q5(A2),

(i) Sketch the small-signal gain as a function of V_{in}.

(ii) What is the region where the gain is zero is commonly known as?

(iii) Suppose we apply a sinusoid with a peak amplitude of 4V to Fig. Q5(A1), sketch the output waveform. Assume V_{BE} = 0.6V.

(iv) The distortion in the output waveform due to zero gain is commonly known as?

(v) How do we avoid, distortion in the output due to zero gain?

5B. For the CB stage shown in Fig. Q5(B), using Miller's theorem, estimate the overall voltage gain. Assume r_O is large enough to allow the approximation $v_{out}/v_X = g_m R_C$

5C. Calculate the closed-loop gain of the circuit in Fig. Q5(C). Assume the Opamp to be ideal with no input current and $\lambda = 0$ for the MOSFET.

(5+3+2)

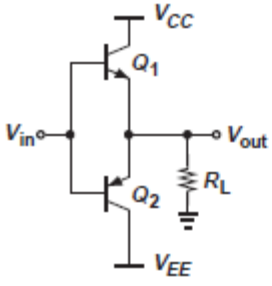

Fig. Q5(A1)

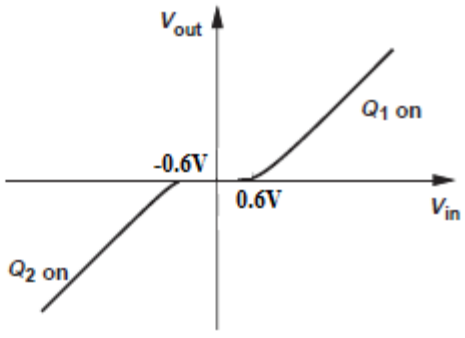

Fig. Q5(A2)

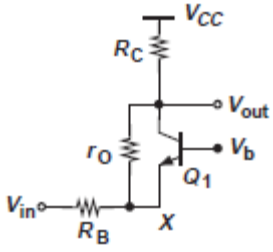

Fig. Q5(B)