Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
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A Constituent Institution of Manipal University

THIRD SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION
NOV 2017
SUBJECT: ANALOG ELECTRONIC CIRCUITS (ECE - 2101)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. A CE stage exhibits a voltage gain of 20 and an output resistance of 1 kΩ. Determine the voltage gain of the CE amplifier if (a) The stage drives an 8Ω speaker directly. (b) An emitter follower biased at a current of 5 mA is interposed between the CE stage and the speaker. Assume $\beta = 100$, $V_A = \infty$, and the follower is biased with an ideal current source.

1B. Determine input/output impedances for the circuit shown in Fig.Q1B. Assume $V_A = \infty$.

1C. A transistor is biased at a collector current of 1 mA. Determine small-signal model if $\beta = 100$ and $V_A = 15$ V.

(5+3+2)

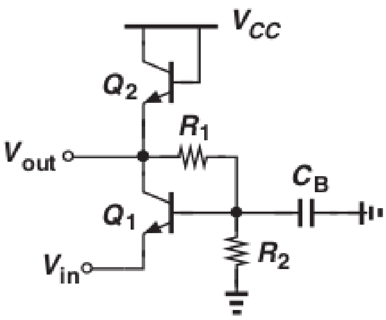

Fig Q1(B).

2A. Determine i) Input resistance ii) Output resistance iii) Voltage gain for the circuit shown in Fig.Q2A. Assume I_D=1mA, V_{DD}=1.8V, V_{TH}=0.4V, $\mu_n C_{OX}$=100μA/V^2, W/L=20, λ =0.

2B. Determine I_D and V_{DS} for the circuit shown in Fig.Q2B. Assume V_{DD}=1.8V, V_{TH}=0.4V, $\mu_n C_{OX}$=100μA/V^2, W/L=20, λ =0.

2C. Draw the small signal equivalent circuit for the circuit shown in Fig.Q2C. Consider Early effect.

(5+3+2)

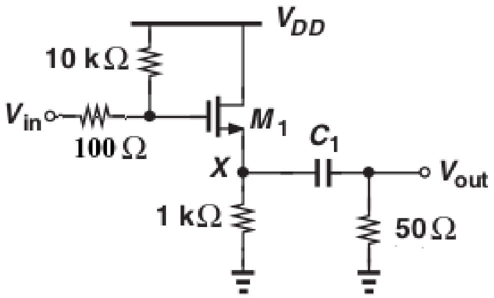

Fig Q2(A)

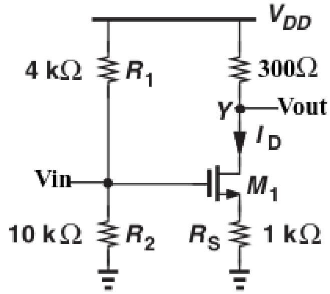

Fig Q2(B)

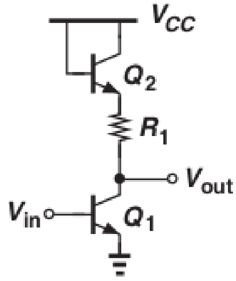

Fig Q2(C).

3A. Design an amplifier using MOSFET with a power budget of 2mW and input impedance of 30kΩ which provides a voltage gain of 7. Assume voltage drop across R_S as 0.3V, V_{DD}=1.8V, V_{TH}=0.4V, $\mu_n C_{OX}$=100μA/V^2, λ =0.

3B. The circuit of Fig. Q3B must be designed for a voltage drop of 200 mV across R_S. (a) Calculate the minimum allowable value of W/L if M_1 must remain in saturation. (b) What are the required values of R_1 and R_2 if the input impedance must be at least 30 kΩ?

3C. A MOSFET carries a drain current of 1 mA with V_{DS}=0.5V in saturation. Determine the change in I_D if V_{DS} rises to 1V and λ=0.1V^{-1}. What is the device output impedance?

(5+3+2)

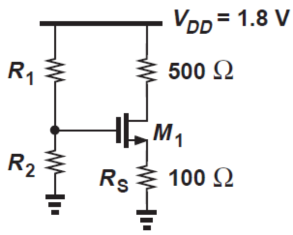

Fig Q3(B).

4A. In the network of Fig. Q4(A1),

(i) With R_1 = R_2 = R and C_1 =C_2 =C, obtain an expression for the transfer function.

(ii) Determine the frequency at which the phase falls to zero.

(iii) If this network is placed around an op amp as in Fig. Q4(A2) and by denoting the gain of the non-inverting amplifier by 'A', determine the minimum value of gain 'A' for sustained oscillation.

(iv) For sustained oscillation, what should be the relationship between R_{F1} and R_{F2}?

(v) Incorporating diodes, redraw the circuit to avoid uncontrolled amplitude growth.

4B. Consider an open-loop amplifier with a transfer function $A(s) = \frac{A_0}{1+\frac{s}{\omega_0}}$

The system is converted into a closed loop system with a feedback factor 'K'. Prove that the unity-gain bandwidth of the closed system remains independent of K if 1 + KA_0 >> 1 and K^2 << 1.

4C. In the amplifier of Fig. Q4(C), R_D = 1kΩ and C_L = 1pF. With λ=0 and junction capacitors neglected, Plot the frequency response, and determine the frequency at which the voltage gain falls by 3dB.

(5+3+2)

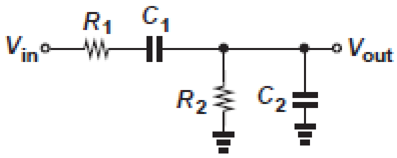

Fig. Q4(A1)

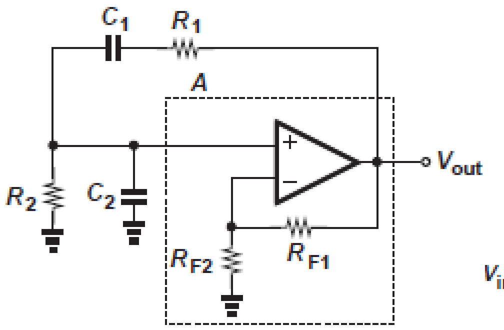

Fig. Q4(A2)

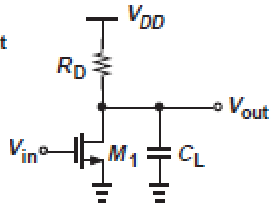

Fig. Q4(C)

5A. For the block diagram shown in Fig. Q5(A1),

(i) Identify the type of the feedback amplifier

(ii) Derive an expression for the closed loop gain I_{out}/I_{in}

(iii) Derive an expression for the input impedance

(iv) Derive an expression for the output impedance

(v) Is the type of feedback amplifier in Fig. 5(A2) is same as that of Fig. Q5(A1)?

5B. In the emitter follower stage shown in Fig. Q5(B), assume $\lambda = 0$, voltage gain = 0.7 and $R_L = 4\Omega$.
(i) At what load current Q_1 turns off?

(ii) For a sinusoidal input, estimate the largest average power that can be delivered to the load without turning Q_1 off.

5C. (i) In a simple push-pull stage, the zone, at which neither transistor conducts and the small-signal gain falls to zero is known as ___.

(ii) ____ amplifier has highest power conversion efficiency.

(iii) Transformer coupled amplifier has a peak power efficiency of ___.

(iv) An amplifier in which the device is ON for the entire cycle is called an ____ amplifier.

(5+3+2)

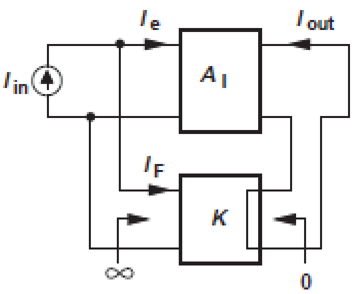

Fig. Q5(A1)

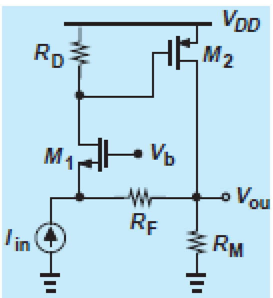

Fig. Q5(A2)

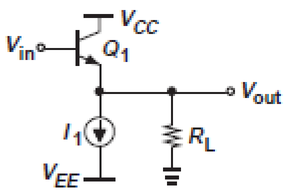

Fig. Q5(B)