



### THIRD SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION

NOV/DEC 2017

SUBJECT: LOGIC DESIGN (ECE - 2105)

TIME: 3 HOURS

MAX. MARKS: 50

#### Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Design a synchronous counter using T flip-flops to count the sequence 0, 1, 2, 5, 7 and repeat. All unused states must go to 2.

1B. Find the minimal product(POS) expression for the function

$$F(a, b, c, d) = \sum m(0, 1, 2, 3, 4, 6, 9, 12, 14) + d(5, 7, 15)$$

1C. Simplify the Boolean expression and implement using NOR gates.

$$F = A + B[AC + (B + \bar{C})D]$$

(5+3+2)

2A. Design a Mealy type sequence detector using T flip-flops to detect an overlapping sequence 1010 using D flip-flop.

2B. Find minimal sum(SOP) expression for the function  $F(w, x, y, z) = \sum m(0, 5, 6, 7, 9, 13, 14, 15)$  using Quine Mc-Cluskey method.

2C. Implement a full adder using a 4:1 MUX.

(5+3+2)

3A. Design Excess-3 to 8421 code converter using active low 4 to 16 decoder.

3B. Design a positive edge triggered asynchronous decade counter using JK flip-flop.

3C. An n bit shift register is fed with an n bit data. Write the number of clock pulses required to shift n bit data out of the shift register if it is a (i) SISO (ii) PISO shift register.

(5+3+2)

4A. Design a 3-bit odd parity generator/checker.

4B. Draw the ASM chart for a mod-6 up-down counter.

4C. Convert the D flip-flop to T flip-flop

(5+3+2)

- 5A. Write Excitation table, Transition Table, State table, Flow table and Flow diagram for the following asynchronous sequential circuit which has two inputs x, y, two SR flip-flops and one output Z.

$$S_1 = x\overline{Q_2}$$

$$R_1 = xQ_2$$

$$S_2 = xyQ_1$$

$$R_2 = \overline{x}\overline{y} + \overline{x}\overline{Q_1}$$

$$Z = x\overline{Q_2} + Q_1\overline{Q_2}$$

- 5B. Define the following i) Fan out ii) Noise Margin iii) Propagation Delay.  
5C. Draw the circuit of a 4-bit Johnson counter and write its truth table.

(5+3+2)